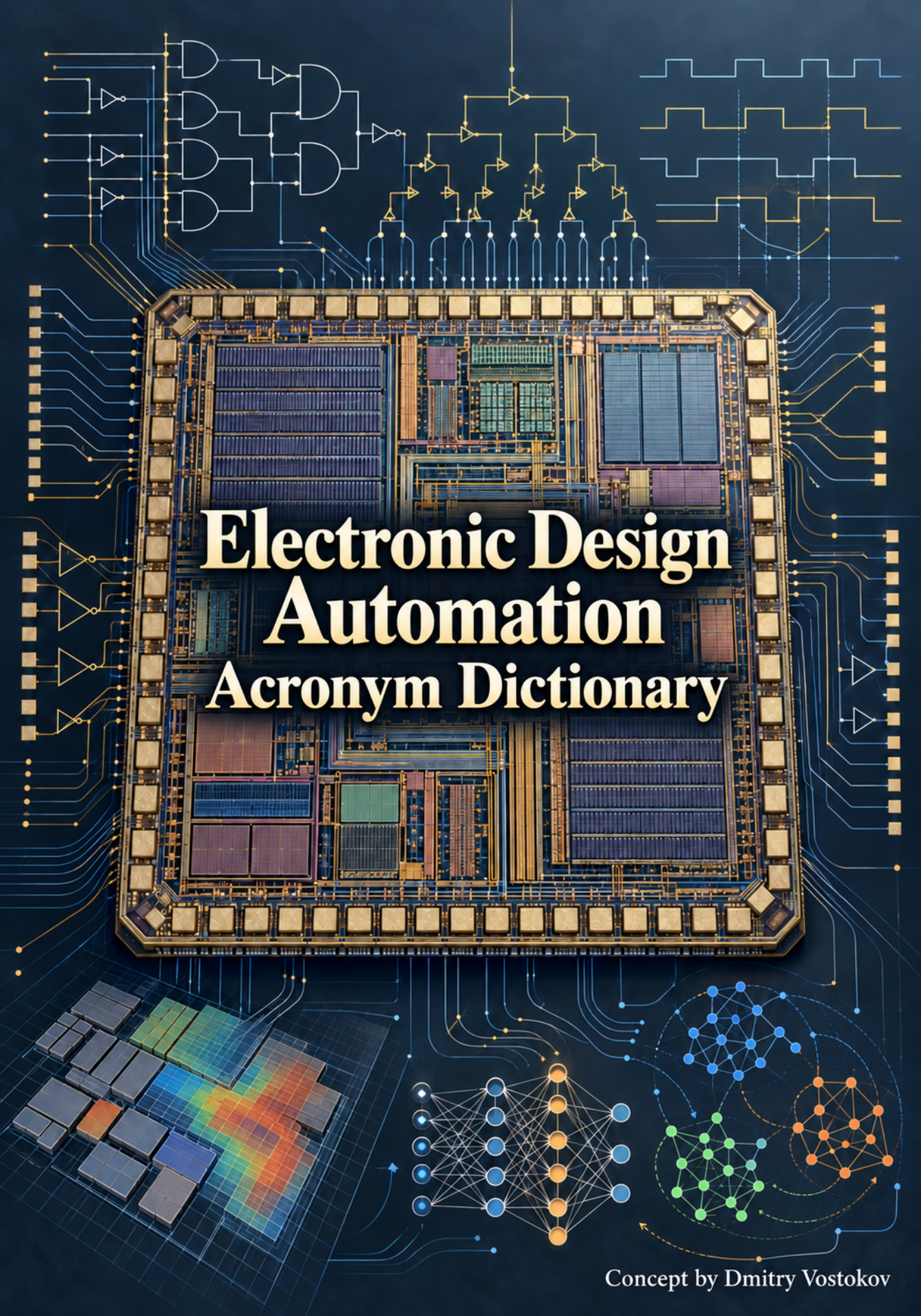




Electronic Design Automation Acronym Dictionary

Concept by Dmitry Vostokov

Electronic Design Automation Acronym Dictionary

Design Verification Implementation Silicon Systems

1,474 entries • 1,379 distinct headwords • 21 domains

Version 7

21 October 2026

This dictionary connects the abbreviations used in electronic design automation with the engineering activities, models, files, interfaces, and physical technologies they describe. It spans the route from system architecture and RTL to implementation, fabrication, test, packaging, and operation, including optimization, AI-assisted design, and photonics.

Each entry gives an expansion or official name, a domain tag, and a concise explanation. Different meanings are recorded separately. Selected symbols, file suffixes, product names, and conventional shorthand are included because they appear alongside acronyms in EDA documentation.

Find a term

[Numbers](#) [A](#) [B](#) [C](#) [D](#) [E](#) [F](#) [G](#) [H](#) [I](#) [J](#) [K](#) [L](#) [M](#) [N](#) [O](#) [P](#) [Q](#) [R](#) [S](#) [T](#) [U](#) [V](#) [W](#) [X](#) [Y](#) [Z](#)

[Ambiguity guide](#) [Domain index](#) [Standards and formats](#) [Primary references](#)

Reading conventions

Entries are ordered by headword, ignoring punctuation for sorting. Capitalization is retained where it helps distinguish names such as SIP and SiP, or SOIC and SoIC. An abbreviation can have several meanings even within one domain. The domain tag and explanation resolve the intended sense. Each entry has one primary tag; uses may span several domains.

An expansion is a name, not a complete definition. Timing reports, test-coverage calculations, corner names, and vendor file formats require the relevant tool, process, or standard conventions. Where naming is local or historical, the entry says so. Product-name expansions are given when documented; historical expansions are marked.

The 94 primary references provide standards anchors, selected terminology checks, and further reading by domain. The explanations are original editorial summaries. Domain references are reading guides, not claims that every entry appears in every listed source. Relevant standards, tool manuals, and process documentation govern implementation details.

Electronic Design Automation Acronym Dictionary

Concept by Dmitry Vostokov

Developed with AI assistance (GPT-6 Astra and Claude Fable 5.1)

Published by OpenTask, Republic of Ireland

Copyright © 2026 by Dmitry Vostokov

Copyright © 2026 by OpenTask

ISBN-13: 978-1-919135-05-2

All rights reserved. No part of this book may be reproduced, stored in a retrieval system, or transmitted in any form or by any means without the publisher's prior written permission.

Product and company names mentioned in this book may be trademarks of their owners.

OpenTask books are available through booksellers and distributors worldwide. For further information or comments, send requests to press@opentask.com.

Version 7

October 2026

Coverage and domain tags

Tag	Coverage	Entries
Core	Foundations and design flow	52
Languages	Languages formats and design databases	72
Verification	Functional verification and simulation	59
Formal	Formal methods and logic synthesis	48
Timing	Timing and library characterization	61
Physical	Physical implementation and signoff	57
Power	Power intent and power management	47
Analog RF	Analog mixed signal and RF	112
Devices	Semiconductor devices and compact models	73
Fabrication	Fabrication lithography and metrology	71
Test	Design for test and silicon debug	92
Reliability	Reliability safety and hardware security	76
Packaging	Packaging chiplets and heterogeneous integration	61
PCB SI	PCB signal integrity and electromagnetic analysis	85
Interfaces	Interfaces protocols and on chip interconnect	98
Architecture	Processors architecture and memory	98
FPGA	FPGA and programmable logic	47
Optimization	Optimization methods for EDA	49
AI/ML	AI ML and supporting numerical methods for EDA	103
Photonics	Photonics MEMS and multiphysics	44
Ecosystem	Tools infrastructure organizations and conferences	69

The counts distinguish meanings, so a headword with several meanings contributes several entries. Alternate spellings and selected named technologies are included in the entry count. The ambiguity guide contains the 82 headwords with more than one recorded meaning; case-sensitive near-collisions are discussed separately.

Alphabetical dictionary

Numbers

2.5D Two-and-a-half-dimensional integration

Packaging. Side-by-side die integration using a high-density interposer or bridge structure.

3D-IC Three-dimensional integrated circuit

Packaging. Integrated circuit using vertically stacked and interconnected active tiers or dies.

3DIC Three-dimensional integrated circuit

Packaging. Alternative spelling of 3D-IC.

A

ABB Adaptive body bias

Power. Dynamic adjustment of transistor body bias to manage speed and leakage.

ABC ABC logic synthesis and verification system

Formal. Berkeley synthesis and verification tool name; no forced acronym expansion.

ABIST Analog built-in self-test

Test. Built-in stimulus and response analysis for analog circuits.

ABIST Array built-in self-test

Test. Built-in testing of memory arrays; terminology varies by vendor.

ABV Assertion-based verification

Verification. Verification approach that expresses intended behavior as executable or provable properties.

AC Alternating current

Analog RF. Time-varying electrical quantity; also denotes small-signal frequency-domain circuit analysis.

ACE AXI coherency extensions

Interfaces. AMBA extensions adding cache-coherency signaling to AXI.

ACLR Adjacent-channel leakage ratio

Analog RF. Ratio quantifying unwanted power leaking into adjacent channels.

ACPR Adjacent-channel power ratio

Analog RF. Adjacent-channel power metric whose exact normalization follows the measurement convention.

AD Automatic differentiation

AI/ML. Algorithmic computation of derivatives through a program's operations.

ADC Analog-to-digital converter

Analog RF. Circuit converting an analog quantity into a digital representation.

ADE Analog design environment

Ecosystem. Cadence analog simulation setup, exploration, and analysis environment.

ADK Assembly design kit

Core. Packaging and assembly design rules, models, and technology data.

ADMM Alternating direction method of multipliers

Optimization. Decomposition method coordinating subproblems with multiplier updates; useful in distributed or decomposed EDA optimization formulations.

ADPLL All-digital phase-locked loop

Analog RF. PLL using predominantly digital phase detection and loop control.

ADS Advanced design system

Ecosystem. Keysight RF and microwave design and simulation environment.

AE Autoencoder

AI/ML. Model learning to reconstruct input through an intermediate representation.

AFM Atomic force microscopy

Fabrication. Surface measurement using probe-sample forces.

AG Assume-guarantee

Formal. Compositional reasoning in which assumptions about an environment support guarantees about a component.

AGC Automatic gain control

Analog RF. Feedback system adjusting gain to maintain a target signal level.

AGU Address generation unit

Architecture. Circuit computing memory addresses for load and store operations.

AHB Advanced high-performance bus

Interfaces. Arm AMBA shared-bus interface family.

AI Artificial intelligence

AI/ML. Computational learning, reasoning, and search methods applied to design automation, verification, and engineering assistance.

AIB Advanced interface bus

Packaging. Die-to-die interface architecture originally developed by Intel.

AIG And-inverter graph

Formal. Logic graph constructed from two-input AND nodes and complemented edges.

AIMC Analog in-memory computing

Architecture. Computation using analog behavior of memory arrays and peripheral circuits.

AiP Antenna in package

Packaging. Integration of antenna structures into an electronic package.

AL Active learning

AI/ML. Selection of informative designs for labeling or simulation, reducing the data cost of EDA prediction and surrogate models.

ALAP As late as possible

Formal. Scheduling strategy assigning operations their latest allowable times.

ALD Atomic layer deposition

Fabrication. Thin-film deposition using sequential self-limiting surface reactions.

ALE Atomic layer etching

Fabrication. Cyclic etching designed for highly controlled removal at atomic-scale increments.

ALF Advanced library format

Languages. Library modeling format historically standardized by IEEE 1603.

ALM Adaptive logic module

FPGA. Altera FPGA logic building block containing configurable logic and registers.

ALU Arithmetic logic unit

Architecture. Circuit performing arithmetic and Boolean operations.

AMBA Advanced microcontroller bus architecture

Interfaces. Arm family of on-chip interface specifications.

AMG Algebraic multigrid

AI/ML. Multilevel solution method constructing coarse levels from algebraic system information.

AMI Algorithmic modeling interface

PCB SI. IBIS interface for executable signal-processing models; specify IBIS context.

AMS Analog and mixed-signal

Analog RF. Circuitry or modeling combining continuous-valued analog behavior with digital behavior.

AMS Designer Analog and mixed-signal Designer

Ecosystem. Cadence mixed-signal simulation product terminology.

ANN Artificial neural network

AI/ML. Expanded abbreviation for a neural-network model.

AO Always on

Power. Circuitry or supply remaining active in the relevant power-management modes.

AOCV Advanced on-chip variation

Timing. Variation model using factors such as path depth and physical distance.

AOI Automated optical inspection

PCB SI. Automated image-based inspection of boards, assemblies, or semiconductor structures.

AON Always on

Power. Common alternative abbreviation for always-on logic or supplies.

APB Advanced peripheral bus

Interfaces. Arm AMBA interface for relatively simple peripheral-register access.

APC Advanced process control

Fabrication. Process adjustment using models, measurements, and feedback or feedforward control.

APD Avalanche photodiode

Photonics. Photodiode using avalanche multiplication to amplify photocurrent.

A-PHY MIPI A-PHY physical layer

Interfaces. MIPI long-reach physical-layer specification aimed at automotive and related links.

API Application programming interface

Languages. Defined callable interface used to access an EDA tool or software component.

APR Automatic place and route

Physical. Automated physical placement and interconnect routing.

ASAP As soon as possible

Formal. Scheduling strategy assigning operations their earliest dependency-respecting times.

ASB Advanced system bus

Interfaces. Historical AMBA system-bus interface.

ASIC Application-specific integrated circuit

Core. Chip designed for a particular application or product rather than general programmability.

ASIL Automotive safety integrity level

Reliability. Risk-based integrity classification used by ISO 26262.

ASIP Application-specific instruction-set processor

Core. Processor with an instruction set tailored to a particular workload.

ASO.ai ASO.ai analog-design optimization product

AI/ML. Synopsys AI product for analog design reuse, optimization, analysis, and layout; the name is retained without an unverified letter-by-letter expansion.

ASP-DAC Asia and South Pacific Design Automation Conference

Ecosystem. Regional EDA research conference.

ASSP Application-specific standard product

Core. Standardized commercial chip serving a class of applications and multiple customers.

AST Abstract syntax tree

Languages. Structured representation of parsed source syntax, omitting unnecessary textual details.

AT Approximately timed

Verification. TLM modeling style exposing more detailed transaction phases and timing.

ATA AT attachment

Interfaces. Storage-interface family named for attachment to the IBM PC AT architecture.

ATB Advanced trace bus

Interfaces. Arm AMBA interface for transporting trace data.

ATDF ASCII test data format

Test. Textual representation associated with semiconductor test-result exchange.

ATE Automatic test equipment

Test. Equipment applying stimuli and measuring device responses in production or characterization.

ATPG Automatic test pattern generation

Test. Algorithmic generation of test patterns targeting modeled circuit faults.

ATS Address translation services

Interfaces. PCIe mechanism allowing devices to request and use address translations.

AU ATPG untestable

Test. Tool classification for faults found untestable under its test constraints or analysis.

AUC Area under the curve

AI/ML. Summary of a specified classifier curve, such as ROC or precision-recall, for hotspot or defect prediction; name the curve explicitly.

AVFS Adaptive voltage and frequency scaling

Power. Feedback-based adjustment of voltage and frequency using silicon or workload observations.

AVS Adaptive voltage scaling

Power. Voltage adjustment based on measured operating conditions or performance margin.

AWE Asymptotic waveform evaluation

AI/ML. Moment-based approximation method for circuit and interconnect transient responses.

AWG Arrayed waveguide grating

Photonics. Photonic wavelength-selective device based on arrays of waveguides with different path lengths.

AWR Applied Wave Research

Ecosystem. Historical company name retained in Cadence AWR RF design product branding.

AXI Advanced extensible interface

Interfaces. Arm AMBA interface family supporting high-performance memory-mapped and streaming communication.

AXI Automated X-ray inspection

PCB SI. Automated internal-structure inspection; distinct from Arm AXI bus terminology.

AXI4-Lite AXI version 4 Lite

Interfaces. Simplified AXI4 memory-mapped interface without burst transfers.

AXI4-Stream AXI version 4 Stream

Interfaces. AXI streaming interface carrying data without memory-address transactions.

B

B2B Back to back

Packaging. Bonding orientation placing die backsides toward each other.

BA Blocking assignment

Verification. Procedural assignment that updates before the following statement proceeds.

BAR Base address register

Interfaces. PCI or PCIe register describing address-space resources exposed by a function.

BAW Bulk acoustic wave

Photonics. Acoustic-wave technology using propagation or resonance within a material body.

B&B Branch and bound

Optimization. Discrete optimization by subdividing a search space and pruning with bounds; used in exact scheduling, allocation, and implementation formulations.

BB Baseband

Analog RF. Signal representation near zero frequency or before carrier modulation.

B&C Branch and cut

Optimization. Branch-and-bound strengthened by valid inequalities, used in mixed-integer formulations of EDA decisions.

BC Best case

Timing. Optimistic analysis condition; which corner is best depends on the metric.

BCD Bipolar CMOS DMOS

Devices. Process integrating bipolar, CMOS, and power DMOS devices.

BDD Binary decision diagram

Formal. Directed graph representing a Boolean function through variable decisions.

BDF Bus device function

Interfaces. Identifier naming a PCI or PCIe function within a hierarchy.

BE Back end

Core. Physical implementation activities such as placement, routing, and signoff; context-dependent.

BEM Boundary element method

PCB SI. Numerical method representing a problem primarily through boundary quantities.

BENCH BENCH netlist format

Languages. Simple logic-netlist format common in academic circuit benchmarks; a format name.

BEOL Back end of line

Core. Wafer processing that forms interconnect layers above devices.

BER Bit error ratio

PCB SI. Fraction of received bits that are erroneous; often informally called bit error rate.

BERT Bit error ratio tester

PCB SI. Instrument generating test data and measuring received bit errors.

BFGS Broyden-Fletcher-Goldfarb-Shanno

Optimization. Quasi-Newton method approximating curvature for smooth optimization, including circuit parameters and differentiable design objectives.

BFM Bus functional model

Verification. Behavioral model driving or responding to bus transactions.

BGA Ball grid array

Packaging. Package using an array of solder balls for external connections.

BGR Bandgap reference

Analog RF. Reference circuit combining temperature-dependent quantities to obtain a stable reference voltage.

BiCMOS Bipolar CMOS

Devices. Process combining bipolar transistors with CMOS devices.

BILBO Built-in logic block observation

Test. Register structure configurable for normal operation, scan, test-pattern generation, and signature analysis.

BIRA Built-in redundancy analysis

Test. On-chip determination of how spare memory resources should repair detected faults.

BISR Built-in self-repair

Test. On-chip repair using spare resources, typically after memory fault detection.

BIST Built-in self-test

Test. On-chip or on-board test generation and response evaluation.

BIT Bitstream file

FPGA. Common FPGA configuration-file extension; not an acronym with one universal expansion.

BJT Bipolar junction transistor

Devices. Transistor using bipolar carrier transport through emitter, base, and collector regions.

BLIF Berkeley logic interchange format

Languages. Text format describing logic networks for synthesis and logic optimization.

BMC Bounded model checking

Formal. Searching for counterexamples within a finite execution depth.

BNF Backus-Naur form

Languages. Grammar notation used to describe language syntax.

BO Bayesian optimization

Optimization. Sequential surrogate-based search for expensive evaluations, including analog sizing and EDA flow tuning.

BoM Bill of materials

Core. Structured list of components and materials needed to build a product.

BoW Bunch of wires

Packaging. Short-reach die-to-die interface architecture associated with the Open Compute Project.

BOX Buried oxide

Devices. Insulating oxide layer beneath the active silicon in SOI structures.

BPF Band-pass filter

Analog RF. Filter passing a selected frequency band.

BPM Beam propagation method

Photonics. Approximate propagation method for optical fields in waveguiding structures.

BPR Buried power rail

Physical. Power conductor embedded near or below device structures rather than occupying conventional upper signal-routing layers.

BRAM Block random-access memory

FPGA. Dedicated embedded RAM block in an FPGA.

BSDL Boundary-scan description language

Test. VHDL-based description of a device's boundary-scan architecture and capabilities.

BSF Band-stop filter

Analog RF. Filter attenuating a selected frequency band.

BSIM Berkeley short-channel IGFET model

Devices. Compact MOS transistor model family.

BSIM-CMG BSIM common multigate

Devices. Compact model for common-gate multigate transistor structures.

BSIM-IMG BSIM independent multigate

Devices. Compact model for independently controlled multigate transistor structures.

BSIM-SOI BSIM silicon on insulator

Devices. Compact model family for SOI MOS devices.

BSPDN Backside power delivery network

Physical. Power distribution implemented on the backside of a wafer or die to separate it from frontside signal routing.

BSR Boundary-scan register

Test. Register connecting boundary-scan cells for observing and controlling chip pins.

BTBT Band-to-band tunneling

Devices. Carrier tunneling between valence and conduction bands.

BTI Bias temperature instability

Reliability. Transistor-parameter drift caused by electrical bias and temperature stress.

BUFG Global clock buffer

FPGA. AMD/Xilinx global clock-distribution primitive name.

BUFGCE Global clock buffer with clock enable

FPGA. AMD/Xilinx clock-buffer primitive supporting clock enable.

BUFR Regional clock buffer

FPGA. AMD/Xilinx regional clock-distribution primitive name.

BUJ Bounded uncorrelated jitter

PCB SI. Bounded jitter component modeled as uncorrelated with the data pattern.

BW Bandwidth

Analog RF. Frequency span over which a circuit meets a defined response criterion.

C**C2C** Chip to chip

Packaging. Communication or physical connectivity between chips.

C4 Controlled collapse chip connection

Packaging. Flip-chip solder-bump interconnection technology and related terminology.

CA Command and address

Architecture. Memory-interface signals or bus carrying command and address information.

CAD Computer-aided design

Core. Computer assistance for design creation, modification, analysis, and documentation.

CAE Computer-aided engineering

Core. Computer-based engineering analysis and simulation supporting design decisions.

CAM Computer-aided manufacturing

Core. Software preparation and control of manufacturing operations from design data.

CAM Content-addressable memory

Architecture. Memory searched by data content rather than solely by an address.

CAN Controller area network

Interfaces. Message-based communication bus used in automotive and industrial systems.

CAN FD CAN with flexible data rate

Interfaces. CAN extension supporting larger payloads and a faster data phase.

CC Code coverage

Verification. Measurement of exercised source constructs, such as statements, branches, or expressions.

CCB Channel-connected block

Timing. Transistor network connected through source/drain terminals, used in circuit timing analysis.

CCF Common-cause failure

Reliability. Multiple failures arising from a shared cause.

CCI Camera control interface

Interfaces. MIPI camera-control interface associated with CSI specifications.

CCI Configuration control and inspection

Languages. Accellera SystemC interfaces for model configuration, control, and introspection; distinct from camera control interface.

CCIX Cache coherent interconnect for accelerators

Interfaces. Coherent interconnect architecture for heterogeneous computing.

CCM Continuous conduction mode

Analog RF. Converter mode in which the relevant inductor current remains nonzero throughout the cycle.

CCOpt Clock concurrent optimization

Physical. Cadence terminology for joint clock-network and timing optimization.

CCS Camera command set

Interfaces. MIPI specification standardizing camera control and discovery; distinct from composite current source.

CCS Composite current source

Timing. Current-source-based library modeling family used for timing, noise, and related analysis.

CD Continuous delivery

Ecosystem. Automation preparing validated changes for release; distinguish critical dimension.

CD Critical dimension

Fabrication. Size of a feature important to device or process performance.

CDC Clock-domain crossing

Verification. Signal transfer between clock domains requiring appropriate synchronization or protocol treatment.

CDFG Control and dataflow graph

Formal. Representation combining control decisions and data dependencies for synthesis.

CDL Circuit description language

Languages. SPICE-like netlist dialect commonly used in physical verification flows.

CDM Charged device model

Reliability. ESD model representing discharge from a charged device.

CDR Clock and data recovery

Analog RF. Recovery of timing and data from a received serial signal.

CD-SEM Critical-dimension scanning electron microscope

Fabrication. SEM specialized for measuring patterned feature dimensions.

CDU Critical-dimension uniformity

Fabrication. Variation of critical dimension across a specified spatial or sample population.

CDV Coverage-driven verification

Verification. Verification process guided by progress toward defined coverage goals.

CEC Combinational equivalence checking

Formal. Equivalence checking treating corresponding combinational inputs and outputs.

CEGAR Counterexample-guided abstraction refinement

Formal. Iterative refinement of an abstract model using spurious counterexamples.

CET Capacitance-equivalent thickness

Devices. Thickness inferred from measured capacitance, including relevant electrical effects.

CEX Counterexample

Formal. Trace demonstrating violation of a property or an equivalence condition.

CFD Computational fluid dynamics

Photonics. Numerical fluid-flow analysis, relevant to cooling and thermal-system design.

CFET Complementary field-effect transistor

Devices. Vertically stacked complementary n-channel and p-channel transistor arrangement.

CFG Control-flow graph

Formal. Graph of possible control transfers between program or behavioral-model blocks.

CG Clock gating

Power. Suppression of unnecessary clock transitions to reduce switching power.

CG Conjugate gradient

Optimization. Iterative method for suitable linear systems and optimization problems; used in quadratic placement and numerical EDA solvers.

CGP Contacted gate pitch

Devices. Pitch between contacted gate structures; often discussed alongside CPP.

CGRA Coarse-grained reconfigurable array

FPGA. Programmable array of larger arithmetic or processing elements rather than fine-grained Boolean cells.

CHI Coherent hub interface

Interfaces. Arm AMBA protocol supporting scalable coherent interconnects.

CHI C2C Coherent hub interface chip to chip

Interfaces. Extension of AMBA CHI concepts across chip boundaries.

CHT Conjugate heat transfer

Photonics. Coupled heat-transfer analysis across solid and fluid regions.

CI Continuous integration

Ecosystem. Frequent automated integration and checking of design or software changes.

CIF Caltech intermediate form

Languages. Textual integrated-circuit layout interchange format, mainly associated with older flows.

CIM Compute in memory

Architecture. Computation performed within or closely integrated with memory arrays to reduce data movement.

CIRCT Circuit IR Compilers and Tools

Languages. LLVM-associated compiler infrastructure applying MLIR to hardware design and compilation.

CISC Complex instruction set computer

Architecture. Processor-design category traditionally associated with richer instruction encodings and operations.

CK Clock

Timing. Alternative clock-pin or signal abbreviation in cell libraries and netlists.

CKE Clock enable

Architecture. Memory control signal affecting clocked operation or power states.

CKQ Clock-to-Q

Timing. Delay from a sequential cell's clock event to its output transition.

CLB Configurable logic block

FPGA. AMD/Xilinx FPGA logic resource grouping lookup tables, registers, and associated logic.

CLI Command-line interface

Ecosystem. Text interface for invoking and scripting EDA operations.

CLK Clock

Timing. Common signal-name abbreviation for a timing reference.

CLM Channel-length modulation

Devices. Effective channel-length variation with drain bias, affecting output conductance.

CMA-ES Covariance matrix adaptation evolution strategy

Optimization. Evolution strategy adapting a search distribution, used for black-box circuit parameters and EDA flow configurations.

Cmax Maximum capacitance corner

Timing. Corner emphasizing high interconnect capacitance; correlations depend on the extraction technology.

CMF Common-mode failure

Reliability. Failures exhibiting a common mode; usage may overlap, but is not identical to, common cause.

CMFB Common-mode feedback

Analog RF. Feedback controlling a differential circuit's common-mode operating level.

Cmin Minimum capacitance corner

Timing. Corner emphasizing low interconnect capacitance; correlations depend on the extraction technology.

CML Compact model library

Photonics. Library of component models for photonic circuit simulation; distinct from current-mode logic.

CML Current-mode logic

Interfaces. Logic and signaling style steering current through differential paths.

CMOS Complementary metal-oxide-semiconductor

Devices. Circuit technology combining complementary n-channel and p-channel MOS devices.

CMP Chemical mechanical planarization

Fabrication. Combined chemical and mechanical removal used to planarize surfaces; also called polishing.

CMRR Common-mode rejection ratio

Analog RF. Measure of differential gain relative to common-mode gain.

CNF Conjunctive normal form

Formal. Boolean formula represented as a conjunction of disjunctive clauses.

CNN Convolutional neural network

AI/ML. Neural network using convolutions; used with layout images or grids for tasks such as hotspot and congestion prediction.

cocotb Coroutine-based cosimulation testbench

Verification. Python-based coroutine framework for testing HDL designs.

COI Cone of influence

Formal. Design elements that can affect a selected property, signal, or endpoint.

COM Channel operating margin

PCB SI. Statistical channel-performance metric used in selected high-speed interface specifications.

CoWoS Chip on wafer on substrate

Packaging. TSMC packaging technology family using wafer-level integration followed by substrate assembly.

CP Charge pump

Analog RF. Circuit sourcing or sinking charge; commonly used in PLL loop filters.

CP Chip probing

Test. Wafer-level electrical test before packaging; also called wafer probing or wafer sort.

CP Clock pin

Timing. Library or schematic abbreviation; naming is not universal.

CPA Correlation power analysis

Reliability. Side-channel method correlating measured power with predicted intermediate behavior.

CPF Common power format

Languages. Power-intent format associated with Si2 and Cadence-originated low-power flows.

C-PHY MIPI C-PHY physical layer

Interfaces. MIPI physical-layer specification using three-wire signaling groups; a specification name.

CPI Cycles per instruction

Architecture. Average clock cycles consumed per completed instruction.

CPLD Complex programmable logic device
FPGA. Programmable logic device typically combining multiple logic blocks with structured interconnect.

CPO Co-packaged optics
Photonics. Optical engines integrated closely with electronic chips within a common package assembly.

CPP Contacted poly pitch
Devices. Device-scaling metric for contacted gate pitch; wording persists even when gate materials are not polysilicon.

CPPR Common-path pessimism removal
Timing. Removal of inconsistent early/late delay treatment on a shared clock-path segment.

CPU Central processing unit
Architecture. Programmable processing unit executing an instruction set.

CPW Coplanar waveguide
PCB SI. Transmission line with signal and adjacent grounds on the same plane.

CQ Clock-to-Q
Timing. Alternative abbreviation for clock-to-output delay.

CRC Cyclic redundancy check
Reliability. Polynomial-based error-detection code widely used in interfaces and stored data.

CRPR Clock reconvergence pessimism removal
Timing. Removal of clock-path reconvergence pessimism; terminology overlaps CPPR across tools.

CRTP Curiously recurring template pattern
Verification. C++ pattern encountered in modeling and simulation infrastructure.

CRV Constrained-random verification
Verification. Randomized stimulus generation restricted by legal-input or scenario constraints.

CSAM C-mode scanning acoustic microscopy

Packaging. Acoustic imaging mode producing planar maps of internal package features.

CSI Camera serial interface
Interfaces. MIPI interface family for camera data.

CSP Chip-scale package
Packaging. Package with dimensions close to the die size, under a specified definition.

CSR Control and status register
Architecture. Register exposing processor or peripheral control and status information.

CST Computer Simulation Technology
Ecosystem. Historical company name retained in Dassault Systèmes electromagnetic simulation branding.

CSV Comma-separated values
Languages. Tabular text exchange format used for reports, measurements, and design metrics.

CTAT Complementary to absolute temperature
Analog RF. Common shorthand for a quantity decreasing with temperature, used in reference circuits.

CTE Coefficient of thermal expansion
Packaging. Fractional dimensional change per temperature change, important for package stress.

CTI Comparative tracking index
Packaging. Material resistance to electrical tracking, relevant to insulation and substrate selection.

CTL Computation tree logic
Formal. Temporal logic combining path quantifiers with temporal operators.

CTL Core test language

Test. IEEE 1450.6 extension to STIL for describing core test information and its use in system-on-chip test integration; distinct from computation tree logic.

CTL* Computation tree logic star

Formal. Temporal logic combining linear-time and branching-time expressiveness.

CTLE Continuous-time linear equalizer

PCB SI. Analog linear equalizer compensating channel frequency-dependent loss.

CTO Clock tree optimization

Physical. Optimization of a clock network for timing, power, and physical constraints.

CTS Clock tree synthesis

Physical. Construction and optimization of the physical clock distribution network.

Cu-Cu Copper-to-copper bonding

Packaging. Direct connection between copper structures; material notation rather than an acronym.

CUDA Compute unified device architecture

AI/ML. NVIDIA parallel-computing platform name with a historical expansion.

CVD Chemical vapor deposition

Fabrication. Film deposition through chemical reactions of gaseous precursors.

CWDM Coarse wavelength-division multiplexing

Photonics. WDM using comparatively wider wavelength spacing.

CXL Compute express link

Interfaces. Coherent interconnect architecture supporting processors, accelerators, and memory expansion.

D**D2D** Die to die

Packaging. Communication, connectivity, or assembly between semiconductor dies.

D2W Die to wafer

Packaging. Bonding individual dies to a wafer.

DA Domain adaptation

AI/ML. Adaptation of an ML model to a different design, technology, or data distribution; transfer quality must be evaluated.

DAC Design Automation Conference

Ecosystem. EDA conference; distinct from digital-to-analog converter.

DAC Digital-to-analog converter

Analog RF. Circuit converting a digital code into an analog quantity.

DAE Differential algebraic equation

AI/ML. System combining differential equations and algebraic constraints, common in circuit simulation.

DAG Directed acyclic graph

Formal. Directed graph containing no directed cycle, common in combinational logic representations.

DAPT Domain-adaptive pretraining

AI/ML. Continued language-model training on domain data, such as chip-design documents, code, and engineering records.

DASC Design Automation Standards Committee

Ecosystem. IEEE committee overseeing numerous hardware design, modeling, and verification standards.

DATE Design Automation and Test in Europe

Ecosystem. Conference covering electronic systems design, automation, and testing.

DB Database

Languages. Generic abbreviation; a .db file's actual format depends on the tool.

DBI Data bus inversion

Architecture. Bus encoding that conditionally inverts data to improve switching or signaling behavior.

DBI Direct bond interconnect

Packaging. Hybrid-bonding technology name associated with dielectric and metal bonding.

DBR Distributed Bragg reflector

Photonics. Periodic reflector used in optical filters, lasers, and cavities.

DBU Database unit

Physical. Integer coordinate unit used by a design database or interchange format.

DC Design Compiler

Ecosystem. Synopsys synthesis product shorthand; distinct from direct current and don't care.

DC Diagnostic coverage

Reliability. Proportion of relevant failures detected by a safety mechanism under defined assumptions.

DC Direct current

Analog RF. Constant or steady electrical quantity; also denotes operating-point and DC sweep analysis.

DC Don't care

Formal. Input or output condition that may be treated as irrelevant under stated assumptions.

DCD Duty-cycle distortion

PCB SI. Asymmetry in timing or pulse widths between opposite logic states or transitions.

DCM Digital clock manager

FPGA. Clock-management resource in older Xilinx FPGA families.

DCM Discontinuous conduction mode

Analog RF. Converter mode in which an inductor current reaches zero during each switching cycle.

DCO Digitally controlled oscillator

Analog RF. Oscillator whose frequency is controlled by a digital code.

DCP Design checkpoint

FPGA. AMD/Xilinx stored design state including implementation-related data.

DCP Disciplined convex programming

Optimization. Rules for certifying convex optimization models, including supported circuit-sizing formulations; distinct from an FPGA design checkpoint.

DCT Discrete cosine transform

AI/ML. Transform expressing a sequence using cosine basis functions.

DD Drift diffusion

Devices. Carrier-transport model using drift and diffusion currents.

DDD Displacement damage dose

Reliability. Measure of radiation damage caused by lattice displacement.

DDJ Data-dependent jitter

PCB SI. Jitter correlated with the transmitted data sequence.

DDR Double data rate

Architecture. Transfer on both edges of a clock or strobe; also names SDRAM families.

DE Differential evolution

Optimization. Population-based search using differences between candidate vectors; used to optimize analog circuit parameters.

DEF Design exchange format

Languages. Physical design instance data, including placement, routing, and connectivity information.

DES Discrete-event simulation

Verification. Simulation advancing between timestamped events rather than uniform small time steps.

Df Dissipation factor

PCB SI. Dielectric loss tangent under specified measurement conditions.

DFA Dependent failure analysis

Reliability. Analysis of common-cause and cascading failures affecting independence assumptions.

DFA Design for assembly

PCB SI. Design practices improving assembly feasibility, quality, and cost.

DFA Differential fault analysis

Reliability. Cryptanalytic method exploiting differences caused by injected faults; distinct from dependent failure analysis.

DFB Distributed feedback

Photonics. Laser or optical structure with distributed feedback provided by a grating.

DFD Design for debug

Physical. Design features enabling diagnosis and observation of implementation behavior.

DFD Design for diagnosis

Test. Design features improving fault localization; DFD also commonly means design for debug.

DFE Decision-feedback equalizer

PCB SI. Equalizer using previous symbol decisions to cancel postcursor interference.

DFF D-type flip-flop

FPGA. Flip-flop sampling its data input on a specified clock event.

DFG Dataflow graph

Formal. Graph whose edges describe data dependencies between operations.

DFM Design for manufacturing

Physical. Design practices and analysis improving chip, package, or board manufacturability and robustness.

DFN Dual flat no-lead

Packaging. Leadless package with contact rows primarily on two sides.

DFO Derivative-free optimization

Optimization. Parameter optimization using function evaluations without explicit derivatives, useful when a SPICE or EDA run supplies the objective.

DFR Design for reliability

Physical. Design practices targeting required lifetime and failure behavior.

DFS Dynamic frequency scaling

Power. Runtime adjustment of operating frequency.

DFT Density functional theory

Devices. Electronic-structure method used in materials and device research; distinct from design for test.

DFT Design for testability

Test. Chip or board features and methods enabling effective testing; also commonly expanded as design for test.

DFT Discrete Fourier transform

AI/ML. Frequency-domain transform used in signal processing and spectral analysis; distinct from design for test.

DFV Design for verification

Physical. Design practices that simplify or strengthen verification.

DFX Design for X

Physical. Umbrella term for design objectives such as test, manufacturing, reliability, or debug.

DFX Dynamic function exchange

FPGA. AMD terminology for supported partial-reconfiguration flows; distinct from design for X.

DFY Design for yield

Physical. Design optimization targeting manufacturing yield.

DIBL Drain-induced barrier lowering

Devices. Reduction of a MOS source-channel barrier with increased drain bias.

DICE Dual interlocked storage cell

Reliability. Storage-cell topology designed to improve tolerance to certain single-node upsets.

DIMM Dual in-line memory module

Architecture. Memory module with separate electrical contacts on its two sides.

DIP Dual in-line package

Packaging. Package with two parallel rows of leads.

DIR Dynamic IR drop

Physical. Time-varying supply drop computed using transient current behavior.

DJ Deterministic jitter

PCB SI. Timing variation associated with bounded or repeatable mechanisms under the selected jitter model.

DK Design kit

Core. General abbreviation for a technology-specific collection of design-enabling data and tools.

Dk Dielectric constant

PCB SI. Common PCB shorthand for relative permittivity under specified measurement conditions.

DL Deep learning

AI/ML. Machine learning using neural networks with multiple learned transformation layers.

DL Defect level

Test. Fraction of defective devices among accepted or shipped devices under a defined model.

DLL Delay-locked loop

Analog RF. Feedback system adjusting delay to align signal phases without a free-running oscillator loop.

DLLP Data link layer packet

Interfaces. PCIe packet carrying data-link control information.

DMA Direct memory access

Architecture. Transfer of data by a device or controller without CPU handling of every data item.

DMI Direct memory interface

Verification. TLM mechanism allowing direct memory access while bypassing repeated transport calls.

DMOS Double-diffused MOS

Devices. MOS transistor structure commonly used for power devices.

DMR Dual modular redundancy

Reliability. Two replicas used to detect disagreement, usually without inherent majority correction.

DMS Digital mixed-signal

Analog RF. Verification approach using event-driven abstractions of analog behavior.

DMSA Distributed multi-scenario analysis

Timing. Timing analysis distributed across multiple scenario workers.

DNF Disjunctive normal form

Formal. Boolean formula represented as a disjunction of conjunctive terms.

DNL Differential nonlinearity

Analog RF. Deviation of a converter code-step width from its ideal value.

DNN Deep neural network

AI/ML. Neural network with multiple learned layers.

DOE Design of experiments

Fabrication. Structured selection of experimental conditions to estimate effects and interactions.

DOF Depth of focus

Fabrication. Allowed focus range over which pattern imaging meets specified requirements.

DP DisplayPort

Interfaces. Digital display interface standardized by VESA; a name rather than a literal acronym expansion.

DP Double patterning

Fabrication. Patterning strategy splitting a target pattern across two patterning operations.

DP Dynamic programming

Optimization. Optimization through linked subproblems; used in buffering, sizing, scheduling, and related design decisions.

DPA Differential power analysis

Reliability. Statistical attack or evaluation using power-trace differences correlated with data hypotheses.

D-PHY MIPI D-PHY physical layer

Interfaces. MIPI short-reach physical-layer specification; D is not expanded here.

DPI Direct programming interface

Languages. SystemVerilog interface for calling foreign-language code, commonly C or C++.

DPI-C Direct programming interface for C

Languages. SystemVerilog foreign-language interface using the C-compatible calling convention.

DPMO Defects per million opportunities

Test. Defect count normalized to one million defined defect opportunities.

DPPM Defective parts per million

Test. Number of defective parts normalized to one million parts.

DPT Double-patterning technology

Fabrication. Technology family using two patterning steps or complementary pattern multiplication approaches.

DPU Data processing unit

Architecture. Processor for data movement, networking, security, or infrastructure offload; vendor scope varies.

DQ Data input and output

Architecture. Memory-interface data signal designation; exact naming follows the interface specification.

DQN Deep Q-network

AI/ML. Deep action-value method for discrete decisions, relevant to selecting synthesis or design actions in learning-based search.

DQS Data strobe

Architecture. Strobe associated with data timing on interfaces such as DDR memory.

DR Data register

Test. Register accessed through a selected JTAG instruction; distinct from detailed routing.

DR Detailed routing

Physical. Assignment of exact tracks, wires, and vias satisfying routing rules.

DRAM Dynamic random-access memory

Architecture. Memory storing charge that requires periodic refresh.

DRC Design rule checking

Physical. Checking layout geometry against specified manufacturing or implementation rules.

DRD Design rule driven

Physical. Layout editing or generation guided by design-rule awareness.

DRIE Deep reactive ion etching

Fabrication. Reactive ion etching used to create deep, high-aspect-ratio structures.

DRL Deep reinforcement learning

AI/ML. Reinforcement learning using deep models, studied for placement and analog circuit-design decisions.

DRM Design rule manual

Physical. Foundry or technology document specifying design constraints and manufacturing rules.

DRMAA Distributed resource management application API

Ecosystem. Interface standard for submitting and controlling distributed-computing jobs.

DRV Design rule violation

Physical. Violation of a specified rule; may mean electrical implementation limits or geometric rules.

DSA Directed self-assembly

Fabrication. Guided material self-organization used to form nanoscale patterns.

DSC Display stream compression

Interfaces. VESA compression technology used in display interfaces.

DSE Design space exploration

Optimization. Evaluation of alternative architectures, parameters, or implementation choices to identify feasible designs and useful trade-offs.

DSI Display serial interface

Interfaces. MIPI interface family for display data.

DSM Delta-sigma modulator

Analog RF. Alternative name and abbreviation for a sigma-delta modulator.

DSO.ai Design space optimization AI

AI/ML. Synopsys AI application for optimizing implementation choices and results.

DSP Digital signal processing

Architecture. Numerical processing of sampled signals; distinguish the processor meaning.

DSP Digital signal processor

Architecture. Processor specialized for numerical signal-processing workloads.

DSPF Detailed standard parasitic format

Languages. Detailed parasitic netlist format supporting post-layout circuit simulation.

DT Detected fault

Test. ATPG fault classification for a fault detected by the generated pattern set.

DTA Dynamic timing analysis

Timing. Timing assessment using simulated input activity and resulting circuit behavior.

DTCO Design technology co-optimization

Core. Joint optimization of device, process, library, and design choices.

DTI Distributed translation interface

Interfaces. AMBA protocol relating translation components to system memory-management functions.

DUT Design under test

Verification. Design instance being verified or tested.

DUV Deep ultraviolet

Fabrication. Lithography using deep-ultraviolet light, including common 193 nm and 248 nm systems.

DUV Design under verification

Verification. Design instance being verified; often used interchangeably with DUT.

DV Design verification

Verification. Checking that a design satisfies its intended specification.

DVCon Design and Verification Conference

Ecosystem. Conference series focused on design and verification methods, languages, and tools.

DVFS Dynamic voltage and frequency scaling

Power. Runtime adjustment of supply voltage and clock frequency to trade performance against power.

DVS Dynamic voltage scaling

Power. Runtime adjustment of supply voltage.

DWDM Dense wavelength-division multiplexing

Photonics. WDM using closely spaced wavelength channels.

E

EA Evolutionary algorithm

Optimization. Population-based optimization using selection and variation, applied to circuit sizing and design-space exploration.

EAM Electro-absorption modulator

Photonics. Optical modulator using electrically controlled absorption.

EBAC Electron-beam absorbed current

Test. Failure-analysis technique imaging absorbed-current behavior under an electron beam.

EBIC Electron-beam induced current

Test. Technique measuring beam-generated carrier current to study semiconductor structures.

EBL Electron-beam lithography

Fabrication. Pattern writing with an electron beam.

EBLIF Extended Berkeley logic interchange format

Languages. Extended BLIF dialect used in some FPGA and synthesis flows.

EBNF Extended Backus-Naur form

Languages. BNF with additional shorthand for repetition and optional constructs.

EC Edge coupler

Photonics. Optical coupling structure at the edge of a photonic chip.

ECAD Electronic computer-aided design

Core. Computer-aided electrical and electronic design, including circuits, boards, and chips.

ECC Error-correcting code

Reliability. Coding that detects and corrects specified classes of data corruption.

ECL Emitter-coupled logic

Interfaces. High-speed bipolar logic family based on current steering.

ECO Engineering change order

Core. Controlled design modification, often performed late in implementation or after silicon.

ECSM Effective current source model

Timing. Current-source-based cell timing and waveform modeling family.

ED2P Energy-delay-squared product

Power. Energy multiplied by delay squared, emphasizing performance more strongly than EDP.

EDA Electronic design automation

Core. Software methods and tools for designing, verifying, implementing, and analyzing electronic systems.

EDC Error-detecting code

Reliability. Coding intended to detect data corruption without necessarily correcting it.

EDIF Electronic design interchange format

Languages. Standard exchange format for electronic design data, including netlists.

EDP Energy-delay product

Power. Energy per operation multiplied by its delay, used to compare implementations.

eDP Embedded DisplayPort

Interfaces. DisplayPort variant for embedded display connections.

EDS Energy-dispersive spectroscopy

Fabrication. Alternative abbreviation for energy-dispersive X-ray analysis in this context.

EDT Embedded deterministic test

Test. Siemens Tessent test-compression technology using deterministic ATPG patterns.

EDX Energy-dispersive X-ray spectroscopy

Fabrication. Elemental analysis using characteristic X-ray energies.

EEnet Electrical equivalent net

Analog RF. Cadence SystemVerilog nettype and modeling approach for electrical interactions, including loading effects.

EEPROM Electrically erasable

programmable read-only memory
Architecture. Nonvolatile memory electrically erased and programmed.

EFA Electrical failure analysis

Test. Electrical characterization and localization of failure behavior.

eFPGA Embedded field-programmable gate array

FPGA. FPGA fabric integrated as IP within another chip.

eFuse Electrical fuse

Architecture. Electrically programmed fuse used for configuration, identification, or redundancy control.

EHVI Expected hypervolume improvement

Optimization. Acquisition criterion for multiobjective Bayesian optimization, used to select analog sizing experiments that improve the current trade-off set.

EI Expected improvement

Optimization. Acquisition criterion averaging predicted improvement, used to choose the next costly circuit simulation or design-flow evaluation.

EIC Electronic integrated circuit

Photonics. Electronic chip distinguished from a PIC in electronic-photonics integration discussions.

EKV Enz Krummenacher Vittoz

Devices. Charge-based MOS compact model named after its developers.

EM Electromagnetic

PCB SI. Field-based electrical analysis context; distinct from electromigration.

EM Electromigration

Reliability. Material transport driven by electrical current, potentially degrading interconnect reliability.

EMC Electromagnetic compatibility

PCB SI. Ability to operate acceptably without causing or suffering unacceptable electromagnetic interference.

EMC/EMI Electromagnetic compatibility and interference

PCB SI. Combined design and analysis area addressing emissions and susceptibility.

EME Eigenmode expansion

Photonics. Optical simulation method expanding fields in local modal bases.

EMI Electromagnetic interference

PCB SI. Unwanted electromagnetic disturbance affecting equipment or signals.

EMIB Embedded multi-die interconnect bridge

Packaging. Intel packaging technology using local embedded bridges for dense die connections.

EMIR Electromigration and IR drop

Physical. Combined interconnect reliability and supply-voltage-drop analysis.

eMMC Embedded multi-media card
Interfaces. JEDEC embedded managed-flash interface and device architecture.

EMMI Emission microscopy
Test. Detection of light emission from electrically active defects or devices.

EMS Electromagnetic susceptibility
PCB SI. Sensitivity of equipment or circuitry to electromagnetic disturbance.

EMX EMX electromagnetic solver
Ecosystem. Cadence solver product name; no universal acronym expansion is assigned.

ENOB Effective number of bits
Analog RF. Converter resolution inferred from measured noise and distortion under specified conditions.

EOS Electrical overstress
Reliability. Damage or degradation caused by electrical conditions beyond device capability.

EOT End of test
Test. Event or timestamp marking completion of a test operation.

EOT Equivalent oxide thickness
Devices. Thickness of silicon dioxide giving the same capacitance as a specified gate dielectric stack.

EPE Edge-placement error
Fabrication. Deviation of a manufactured or simulated edge from its intended position.

EPIC Electronic-photonic integrated circuit
Photonics. Integrated circuit combining electronic and photonic functions.

EPROM Erasable programmable read-only memory
Architecture. Programmable memory traditionally erased using ultraviolet exposure.

ER Extinction ratio
Photonics. Ratio of optical high-state to low-state power under a specified convention.

ERC Electrical rule checking
Physical. Checking electrical consistency and connection rules beyond purely geometric constraints.

eRM e reuse methodology
Verification. Reusable verification methodology for the e verification language.

ESD Electrostatic discharge
Reliability. Rapid transfer of electrostatic charge that can damage devices.

ESDA ESD Association
Ecosystem. Organization developing electrostatic-discharge standards and guidance; distinguish EDA industry organizations.

ESD Alliance Electronic System Design Alliance
Ecosystem. Industry association representing electronic system design; currently a SEMI technology community.

ESL Electronic system level
Core. System-level modeling and design above detailed RTL implementation.

ESL Equivalent series inductance
Analog RF. Series inductance modeling component and interconnect parasitics; distinct from electronic system level.

ESR Equivalent series resistance
Analog RF. Series resistance used to model loss in a capacitor, inductor, or network.

ETM Extracted timing model
Timing. Timing abstraction derived from a design block for hierarchical analysis.

ETS European Test Symposium
Ecosystem. Conference on electronic test, reliability, and related research.

EUV Extreme ultraviolet

Fabrication. Lithography wavelength regime centered near 13.5 nm in semiconductor production systems.

EVCD Extended value change dump

Languages. VCD extension recording additional information, including port direction and drive strength.

EVM Error vector magnitude

Analog RF. Magnitude of modulation error relative to a defined reference signal.

EXDC External don't care

Formal. Don't-care information supplied externally to a logic network.

F**F2B** Face to back

Packaging. Bonding orientation placing one active face toward another die's backside.

F2F Face to face

Packaging. Bonding orientation placing active faces toward each other.

FA Failure analysis

Test. Investigation of failure mechanisms, locations, and causes.

FastSPICE Fast SPICE simulation

Analog RF. Accelerated circuit-simulation approaches for large designs; accuracy and partitioning depend on implementation.

FBAR Film bulk acoustic resonator

Photonics. Thin-film bulk acoustic-wave resonator.

FBB Forward body bias

Power. Body bias that generally lowers threshold magnitude to increase speed, with leakage implications.

FBGA Fine-pitch ball grid array

Packaging. BGA package with comparatively fine connection pitch.

FC Fault coverage

Test. Fraction of modeled faults detected, subject to stated fault-list and denominator conventions.

FC Functional coverage

Verification. Measurement of whether specified functional scenarios and value combinations have been exercised.

FC Fusion Compiler

Ecosystem. Synopsys implementation product shorthand; distinct from fault and functional coverage.

FCBGA Flip-chip ball grid array

Packaging. BGA package using flip-chip die attachment.

FCO Functional change order

Core. Change affecting intended circuit functionality; local usage may overlap ECO.

FDC Fault detection and classification

Fabrication. Monitoring and classification of equipment or process abnormalities.

FDE Finite-difference eigenmode

Photonics. Numerical mode-solving approach used for waveguides and optical structures.

FD-SOI Fully depleted silicon on insulator

Devices. SOI transistor technology with a fully depleted thin body.

FDTD Finite-difference time-domain method

PCB SI. Time-domain field-solving method based on spatial and temporal finite differences.

FE Front end

Core. Early design activities such as architecture, RTL, and verification; context-dependent.

FEA Finite element analysis

Photonics. Analysis using the finite element method for structural, thermal, electromagnetic, or coupled problems.

FEC Forward error correction

PCB SI. Redundancy allowing a receiver to correct certain transmission errors without retransmission.

FeFET Ferroelectric field-effect transistor

Devices. Transistor incorporating a ferroelectric gate-stack element.

FEM Finite element method

PCB SI. Numerical method commonly used for electromagnetic, thermal, and mechanical analysis.

FEOL Front end of line

Core. Wafer processing that forms transistors and related device structures.

FeRAM Ferroelectric random-access memory

Architecture. Memory using ferroelectric polarization to retain data.

FET Field-effect transistor

Devices. Transistor controlled by an electric field affecting channel conduction.

FEV Formal equivalence verification

Formal. Proof that two design representations agree under the selected equivalence model.

FEXT Far-end crosstalk

PCB SI. Coupled interference observed at the far end of a victim interconnect.

FF Fast-fast process corner

Timing. Corner with fast NMOS and fast PMOS behavior in a specified process convention.

FF Flip-flop

FPGA. Edge-triggered storage element; distinct from fast-fast process corner.

FFE Feed-forward equalizer

PCB SI. Equalizer combining weighted delayed samples or symbols without decision feedback.

FFT Fast Fourier transform

AI/ML. Efficient algorithm family for computing the discrete Fourier transform.

FI Fault injection

Reliability. Deliberate disturbance used to evaluate robustness, safety mechanisms, or security.

FIB Focused ion beam

Fabrication. Ion-beam tool used for sectioning, editing, and specimen preparation.

FIFO First in first out

Architecture. Queue discipline or hardware buffer preserving arrival order.

FinFET Fin field-effect transistor

Devices. Multigate transistor with a fin-shaped channel.

FIR Finite impulse response

PCB SI. Filter whose response to an impulse has finite duration.

FIRRTL Flexible intermediate representation for RTL

Languages. Hardware intermediate representation associated with Chisel and CIRCT compilation flows.

FIT Failures in time

Reliability. Failure-rate unit corresponding to one failure per billion device-hours.

FLI Foreign language interface

Languages. Vendor-specific interface for connecting foreign code to a simulator, often VHDL.

FLIT Flow control unit

Interfaces. Fixed-size link transfer or flow-control unit; format depends on the interconnect.

FLL Frequency-locked loop

Analog RF. Feedback system controlling oscillator frequency relative to a reference.

FLUTE Fast lookup table based wirelength estimation

Physical. Lookup-table-based method for fast rectilinear Steiner-tree and wire-length estimation.

FM Fiduccia-Mattheyses

Optimization. Circuit-partitioning heuristic that moves individual cells and tracks cut-cost gains while maintaining balance constraints.

FM Formality

Ecosystem. Synopsys equivalence-checking product shorthand; expansion depends on context.

FMA Fused multiply-add

Architecture. Operation computing multiplication and addition with a single final rounding.

Fmax Maximum operating frequency

Timing. Highest clock frequency meeting specified timing constraints and operating conditions.

FMEA Failure mode and effects analysis

Reliability. Systematic analysis of failure modes and their consequences.

FMEDA Failure modes effects and diagnostic analysis

Reliability. FMEA extended with diagnostic coverage and failure-rate assessment.

Fmin Minimum operating frequency

Timing. Lowest supported operating frequency when a circuit or interface imposes one.

FMM Fast multipole method

AI/ML. Acceleration technique for selected long-range interaction and field calculations.

FNR False negative rate

AI/ML. Fraction of actual positives missed by a classifier, for example undetected lithography hotspots.

FO Fanout

Timing. Number of loads driven by a signal, or an electrical loading ratio in a specified context.

FO4 Fanout of four

Timing. Delay benchmark using an inverter driving four comparable inverter inputs.

FOPLP Fan-out panel-level packaging

Packaging. Fan-out packaging using a panel rather than a circular wafer carrier.

Foveros Foveros

Packaging. Intel packaging technology family name; not an acronym to expand.

FOWLP Fan-out wafer-level packaging

Packaging. Wafer-level packaging extending connections beyond the die footprint.

FP False path

Timing. Path excluded from a timing check because the specified timing relationship is irrelevant.

FP Floorplanning

Physical. Allocation of chip or block dimensions, macros, interfaces, and major physical resources.

FPGA Field-programmable gate array

FPGA. Integrated circuit with configurable logic and routing resources.

FPR False positive rate

AI/ML. Fraction of actual negatives incorrectly flagged, for example benign layout regions marked as hotspots.

FPU Floating-point unit

Architecture. Circuit performing floating-point arithmetic.

FPV Formal property verification

Formal. Formal analysis of assertions and other behavioral properties.

FRAM Ferroelectric random-access memory

Architecture. Alternative abbreviation for FeRAM, including vendor usage.

FS Fast-slow process corner

Timing. Mixed transistor corner; confirm the foundry's ordering of NMOS and PMOS labels.

FSDB Fast signal database

Languages. Proprietary waveform database format associated with Verdi and related tools.

FSI Fluid-structure interaction

Photonics. Coupled analysis of fluid flow and structural response.

FSL Functional safety language

Languages. Accellera language standard for exchanging functional-safety information across design and analysis flows.

FSM Finite-state machine

Verification. Model composed of a finite set of states and transitions.

FSR Free spectral range

Photonics. Frequency or wavelength spacing between adjacent resonances; distinct from converter full-scale range.

FSR Full-scale range

Analog RF. Analog input or output range represented by a converter.

FST Fast signal trace

Languages. Compact waveform format used by open-source simulation and waveform tools.

FT Final test

Test. Electrical testing of packaged devices before shipment.

FTA Fault tree analysis

Reliability. Top-down analysis of combinations of events leading to a specified failure.

FTTI Fault tolerant time interval

Reliability. Maximum time between a fault and a possible hazardous event under the specified safety analysis.

FV Formal verification

Formal. Mathematical checking of design properties under explicitly stated assumptions.

FV Functional verification

Verification. Validation of intended design behavior; FV also commonly denotes formal verification.

G

GA Genetic algorithm

Optimization. Evolutionary search using selection, crossover, and mutation, applied to discrete and mixed circuit-design choices.

GAA Gate all around

Devices. Transistor geometry with a gate surrounding the channel.

GaAs Gallium arsenide

Devices. Compound semiconductor used in RF, microwave, and optoelectronic devices.

GAL Generic array logic

FPGA. Historical reprogrammable logic-device family compatible with selected PAL functions.

GAN Generative adversarial network

AI/ML. Generative modeling framework training a generator against a discriminator.

GaN Gallium nitride

Devices. Wide-bandgap semiconductor used for power and high-frequency devices.

GAT Graph attention network

AI/ML. Graph neural network using learned attention over neighbors, allowing circuit connections to contribute with different weights.

GBA Graph-based analysis

Timing. Timing propagation through a graph using merged worst-case quantities at nodes.

GBDT Gradient-boosted decision trees

AI/ML. Tree ensemble trained by successive gradient-based boosting steps.

GBW Gain-bandwidth product

Analog RF. Amplifier gain multiplied by corresponding bandwidth under an applicable approximation.

GC Grating coupler

Photonics. Structure coupling light between a waveguide and another optical path through a grating.

GCell Global routing cell

Physical. Spatial bin in the routing grid used for capacity and congestion estimation.

GCN Graph convolutional network

AI/ML. Graph neural network aggregating neighborhood information, used for circuit representations and transistor-sizing policies.

GCPW Grounded coplanar waveguide

PCB SI. Coplanar waveguide with an additional ground plane.

GD Gradient descent

Optimization. Updates design variables along a negative-gradient direction, for example when minimizing a differentiable placement objective.

GDDR Graphics double-data-rate memory

Architecture. High-bandwidth DRAM interface family commonly used with graphics processors.

Gds Drain-source conductance

Devices. Small-signal derivative of drain current with respect to drain-source voltage.

GDSII Graphic Data System II

Languages. Binary layout exchange format; also written GDS2 or GDS II.

GDS-to-silicon GDS layout to manufactured silicon

Core. Flow shorthand for manufacturing from released layout data; not a formal acronym.

GEMM General matrix multiplication

AI/ML. Dense matrix-multiplication operation central to numerical and machine-learning computation.

GenAI Generative artificial intelligence

AI/ML. AI producing candidate code, scripts, text, or design content; generated hardware still requires normal verification.

GIDL Gate-induced drain leakage

Devices. Leakage associated with high electric fields near a gate-drain region.

GIN Graph isomorphism network

AI/ML. GNN architecture with expressive neighborhood aggregation, used to learn structural features of circuits.

GLIFT Gate-level information flow tracking

Reliability. Information-flow tracking applied to gate-level hardware representations.

GLS Gate-level simulation

Verification. Simulation of an implemented gate netlist, optionally with annotated delays.

GM Gain margin

Analog RF. Gain increase available before the selected loop phase condition reaches instability.

Gm Transconductance

Devices. Small-signal derivative of output current with respect to controlling input voltage.

Gm-C Transconductance-capacitance

Analog RF. Analog circuit technique using transconductors and capacitors, commonly for filters.

GMII Gigabit media-independent interface

Interfaces. Parallel interface between gigabit Ethernet MAC and PHY functions.

GMRES Generalized minimal residual

AI/ML. Iterative method for nonsymmetric linear systems.

GNN Graph neural network

AI/ML. Neural network learning from graph structure, including netlists, circuit connectivity, and timing graphs.

GP Gaussian process

AI/ML. Probabilistic model over functions, used as a surrogate for circuit performance or expensive design-flow evaluations.

GP Geometric programming

Optimization. Optimization with posynomial inequalities and monomial equalities, used for suitable circuit-sizing and design-trade-off models.

GPR Gaussian process regression

AI/ML. Regression using a Gaussian-process model, including surrogate prediction of circuit metrics with uncertainty estimates.

GPU Graphics processing unit

Architecture. Highly parallel processor originating in graphics and widely used for computation.

GR Global routing

Physical. Coarse routing that allocates nets to routing regions or guides.

GRU Gated recurrent unit

AI/ML. Gated recurrent-network architecture with a compact state-update structure.

GSA Global Semiconductor Alliance

Ecosystem. Semiconductor industry association.

GT Gigabit transceiver

FPGA. Vendor shorthand for FPGA high-speed serial-transceiver resources.

GUI Graphical user interface

Ecosystem. Visual interface for interacting with designs, settings, and analysis results.

H

HAPS High-performance ASIC prototyping system

Ecosystem. Synopsys FPGA-based ASIC prototyping product family; expansion documented by the vendor.

HAST Highly accelerated stress test

Reliability. Humidity and temperature stress test, often performed under elevated pressure.

HB Harmonic balance

Analog RF. Frequency-domain nonlinear steady-state simulation method.

HB Hybrid bonding

Packaging. Bonding combining dielectric and metal connections; distinct from harmonic balance.

HBI High-bandwidth interconnect

Packaging. General abbreviation for dense interconnect; can also denote vendor-specific interfaces.

HBM High-bandwidth memory

Architecture. Stacked DRAM architecture using wide interfaces; distinct from the ESD human body model.

HBM Human body model

Reliability. ESD test model representing a charged human contacting a device; distinct from high-bandwidth memory.

HBT Heterojunction bipolar transistor

Devices. Bipolar transistor using different semiconductor materials at a junction.

HCD Hot-carrier degradation

Reliability. Device-performance degradation caused by hot-carrier-related mechanisms.

HCI Hot-carrier injection

Reliability. Injection of energetic carriers into insulating regions, potentially causing device degradation.

HD Hydrodynamic

Devices. Carrier-transport modeling including carrier energy or related higher-order moments.

HDI High-density interconnect

PCB SI. PCB technology using fine features, microvias, and dense layer interconnection.

HDL Hardware description language

Core. Language for describing hardware structure and behavior for simulation or synthesis.

HDMI High-definition multimedia interface

Interfaces. Digital interface for audiovisual data and related control.

HEMT High-electron-mobility transistor

Devices. Heterostructure transistor exploiting a high-mobility carrier channel.

HFSS High-frequency structure simulator

Ecosystem. Ansys electromagnetic simulation product name.

HGNN Hypergraph neural network

AI/ML. Learning on hyperedges connecting multiple nodes, matching multi-pin relationships in netlists.

HI Heterogeneous integration

Packaging. Integration of components differing in function, process, technology, or material.

HICUM High-current model

Devices. Compact bipolar transistor model family.

High-NA High numerical aperture

Fabrication. Relative designation for higher-aperture lithography optics; platform context determines the value.

HiSIM Hiroshima University STARC IGFET model

Devices. Surface-potential-based compact transistor model family.

HKMG High-k metal gate

Devices. Gate-stack technology using a high-permittivity dielectric and metal gate electrode.

HLD High-level design

Core. Architectural or behavioral design before detailed implementation; usage varies by organization.

HLS High-level synthesis

Core. Automatic generation of hardware implementations from higher-level behavioral descriptions.

HMC Hybrid memory cube

Architecture. Historical stacked-memory architecture using a logic base and serial links.

HOL Head-of-line blocking

Interfaces. Blocked traffic preventing unrelated following traffic from advancing.

HPC High-performance computing

Ecosystem. Compute infrastructure used for large simulation, extraction, and optimization workloads.

HPF High-pass filter

Analog RF. Filter passing higher frequencies while attenuating lower frequencies.

HPO Hyperparameter optimization

Optimization. Search over model or search-algorithm settings; relevant to EDA predictors and automated tuning workflows.

HPS Hard processor system

FPGA. Processor subsystem integrated with programmable logic in selected Altera SoCs.

HPWL Half-perimeter wire length

Physical. Placement wire-length estimate based on each net's bounding-box half-perimeter.

HRoT Hardware root of trust

Reliability. Root of trust anchored in hardware mechanisms.

HSM Hardware security module

Reliability. Hardware subsystem providing protected cryptographic operations and key management.

HSPICE HSPICE circuit simulator

Ecosystem. Synopsys circuit-simulation product name; do not infer a separate expansion for H.

HSTL High-speed transceiver logic

Interfaces. Low-voltage I/O signaling standard family.

HT Hardware Trojan

Reliability. Malicious hardware modification affecting behavior, leakage, or reliability.

HTGB High-temperature gate bias

Reliability. Reliability stress applying gate bias at elevated temperature.

HTOL High-temperature operating life

Reliability. Accelerated reliability test stressing powered devices at high temperature.

HTRB High-temperature reverse bias

Reliability. Reliability stress applying reverse bias at elevated temperature.

H-tree H-shaped clock distribution tree

Physical. Symmetric clock distribution topology; a topology name rather than an acronym.

HV Hypervolume

Optimization. Volume dominated by a Pareto approximation relative to a reference point; a measure of multiobjective circuit-design trade-offs.

HVL Hardware verification language

Core. Language or language features aimed at constructing verification environments.

HVT High threshold voltage

Power. Device or cell option generally favoring lower leakage over speed.

I

I2C Inter-integrated circuit

Interfaces. Two-wire serial bus using clock and bidirectional data signals.

I2S Inter-IC sound

Interfaces. Serial digital-audio interface; commonly written I²S.

I3C Improved inter-integrated circuit

Interfaces. MIPI serial interface supporting improved performance and features relative to I2C.

IaaS Infrastructure as a service

Ecosystem. Hosted compute, storage, and networking resources supporting tool execution.

IaC Infrastructure as code

Ecosystem. Machine-readable definitions for provisioning compute and supporting services.

IBIS I/O buffer information specification

PCB SI. Behavioral model standard for electronic buffers and associated package information.

IBIS-AMI IBIS algorithmic modeling interface

PCB SI. Interface for algorithmic models of high-speed serial transmitters and receivers.

IBIS-ISS IBIS interconnect SPICE subcircuit
PCB SI. Standardized SPICE-subcircuit subset for interconnect modeling.

IC Integrated circuit
Core. Electronic circuit fabricated as interconnected devices on a semiconductor die.

IC3 Incremental construction of inductive clauses for indubitable correctness
Formal. Property-directed safety-checking algorithm using progressively strengthened clause frames.

ICAP Internal configuration access port
FPGA. Internal FPGA interface to configuration functions in supported AMD/Xilinx devices.

ICC IC Compiler
Ecosystem. Synopsys physical implementation product shorthand.

ICC2 IC Compiler II
Ecosystem. Synopsys physical implementation product shorthand, also written ICC II.

ICCAD International Conference on Computer-Aided Design
Ecosystem. Conference on electronic design automation and related methods.

ICE In-circuit emulation
Verification. Emulation connected to a target system or its real interfaces.

ICG Integrated clock-gating cell
Power. Library cell implementing glitch-controlled clock gating.

ICL In-context learning
AI/ML. Use of examples in an LLM prompt to guide a task such as RTL or EDA-script generation without updating model weights.

ICL Instrument connectivity language
Test. IEEE 1687 language describing embedded-instrument access connectivity.

ICM Interconnect modeling specification
PCB SI. IBIS-associated interconnect model specification.

ICP Inductively coupled plasma
Fabrication. Plasma source using inductive coupling, used in etch and deposition equipment.

ICT In-circuit test
PCB SI. Board test measuring components and connections through accessible test points.

ICV IC Validator
Ecosystem. Synopsys physical-verification product shorthand.

IDDQ Quiescent supply current
Test. Supply-current measurement under stable logic conditions, used for selected defect detection.

IDDT Transient supply current
Test. Time-varying supply-current behavior used in some testing and characterization methods.

IDE Integrated development environment
Ecosystem. Software development interface combining editing, navigation, build, and debug facilities.

IDE Integrity and data encryption
Interfaces. Link security capability in PCIe and related CXL contexts.

IDF Intermediate data format
PCB SI. Exchange format supporting ECAD and mechanical-CAD collaboration for board assemblies.

IDM Integrated device manufacturer
Core. Company combining semiconductor design and manufacturing operations.

Ids Drain-to-source current
Devices. MOS drain-current notation; a symbol rather than an acronym.

IDX Incremental design exchange

PCB SI. Incremental ECAD-MCAD exchange format associated with ProSTEP collaboration workflows.

IEC International Electrotechnical Commission

Ecosystem. Organization developing international electrotechnical standards.

IEDM International Electron Devices Meeting

Ecosystem. Conference on semiconductor devices and process technologies.

IEEE Institute of Electrical and Electronics Engineers

Ecosystem. Professional and standards organization publishing many hardware-language and test standards.

IF Intermediate frequency

Analog RF. Frequency between RF and baseband in a conversion chain.

IFFT Inverse fast Fourier transform

AI/ML. Efficient computation of the inverse discrete Fourier transform.

IFT Information flow tracking

Reliability. Analysis or instrumentation tracking propagation of information through hardware or software.

IGBT Insulated-gate bipolar transistor

Devices. Power device combining MOS gate control with bipolar conduction.

IGFET Insulated-gate field-effect transistor

Devices. FET with an insulated gate; broader term underlying the BSIM expansion.

II Initiation interval

Formal. Number of cycles between successive starts of a pipelined operation or loop iteration.

IIP3 Input third-order intercept point

Analog RF. Third-order intercept referred to the input.

IIR Infinite impulse response

PCB SI. Filter with an impulse response that may persist indefinitely due to feedback.

IJTAG Internal JTAG

Test. Common name for IEEE 1687 access to embedded instruments.

IL Insertion loss

PCB SI. Reduction in transmitted signal power or amplitude caused by inserting a network.

ILA Integrated logic analyzer

FPGA. Embedded FPGA debug instrument for capturing internal signals.

ILM Interface logic model

Timing. Block abstraction retaining interface-relevant logic and timing connectivity.

ILP Integer linear programming

Optimization. Linear optimization with integer variables, used to encode discrete choices in scheduling, mapping, and implementation.

ILT Inverse lithography technology

Fabrication. Optimization of mask patterns by solving an inverse imaging problem.

IMC In-memory computing

Architecture. Computation associated with memory structures; usage overlaps compute in memory.

IMD Intermodulation distortion

Analog RF. Unwanted frequency components generated by nonlinear mixing of input tones.

InFO Integrated fan-out

Packaging. TSMC fan-out packaging technology family.

INL Integral nonlinearity

Analog RF. Deviation of a converter transfer curve from a defined reference line.

I/O Input and output

Timing. Boundary signals or interfaces; used in timing constraints and physical implementation.

IOB Input-output block

FPGA. FPGA resource connecting internal logic to external pins.

IOB Input-output buffer

FPGA. Alternative local expansion for input/output circuitry; distinguish a vendor's block definition.

IOE Input-output element

FPGA. Altera FPGA I/O resource terminology.

IOLOGIC Input-output logic

FPGA. Dedicated FPGA logic associated with I/O registers and serialization.

IOMMU Input-output memory management unit

Architecture. Address translation and protection for device-initiated memory accesses.

IP Integer programming

Optimization. Optimization with integer decision variables, used to encode discrete implementation choices; distinct from intellectual property.

IP Intellectual property

Core. Reusable design content, such as a processor core, interface block, or physical library.

IP2 Second-order intercept point

Analog RF. Extrapolated input or output level where second-order distortion equals fundamental response.

IP3 Third-order intercept point

Analog RF. Extrapolated level where third-order distortion equals fundamental response.

IPC Instructions per cycle

Architecture. Instruction throughput normalized by clock cycles.

IPC Interprocess communication

Ecosystem. Communication between software processes; distinguish instructions per cycle and the standards organization.

IPC IPC standards designation

Ecosystem. Standards brand retained after IPC became the Global Electronics Association in 2025. Earlier names were Institute of Printed Circuits (1957) and Institute for Interconnecting and Packaging Electronic Circuits (1977). Its current history dates the standalone name IPC to 1999; its 2007 chronology lists the change under 1998.

IPC-2581 IPC 2581 electronic product manufacturing description

PCB SI. XML-based manufacturing data exchange standard; IPC is the standards organization's name.

IPC-D-356 IPC D 356 electrical test description

PCB SI. Standard representation of bare-board electrical test information.

IPD Integrated passive device

Packaging. Integrated passive components such as resistors, capacitors, and inductors.

IPSA IP security assurance

Languages. Accellera activity addressing security assurance of hardware IP and its integration.

IP-XACT IP-XACT

Languages. IEEE 1685 XML metadata standard for IP and system integration; retain the official name.

I/Q In-phase and quadrature

Analog RF. Orthogonal signal components used in modulation, demodulation, and modeling.

IR Instruction register

Test. Register selecting a JTAG instruction; also used for processor instruction registers.

IR Intermediate representation

Languages. Internal design representation used between compiler or synthesis transformations.

IR-drop Current times resistance voltage drop

Physical. Supply-voltage loss associated with resistive current flow; IR is symbolic notation.

IRDS International Roadmap for Devices and Systems

Ecosystem. IEEE roadmap initiative covering electronic devices and systems.

ISA Instruction set architecture

Architecture. Software-visible instruction and execution-state contract of a processor.

ISI Intersymbol interference

PCB SI. Distortion causing neighboring symbols to interfere with the current symbol.

ISO International Organization for Standardization

Ecosystem. International standards organization; ISO is its chosen short name rather than a literal English initialism.

ISO Isolation

Power. Control of outputs from a power-down region to prevent invalid values reaching active logic.

ISPD International Symposium on Physical Design

Ecosystem. Conference focused on physical design methods and tools.

ISQED International Symposium on Quality Electronic Design

Ecosystem. Conference addressing electronic design quality and related technologies.

ISS Instruction-set simulator

Verification. Software model executing an architecture's instruction semantics.

ISSCC International Solid-State Circuits Conference

Ecosystem. Conference presenting integrated-circuit design research.

IST In-system test

Test. Testing performed while a component is installed in its system environment.

ITC International Test Conference

Ecosystem. Conference focused on electronic test and related topics.

ITRS International Technology Roadmap for Semiconductors

Ecosystem. Historical semiconductor technology roadmap initiative.

J**JEDEC** Joint Electron Device Engineering Council

Ecosystem. Historical expansion of JEDEC, now the JEDEC Solid State Technology Association.

JFET Junction field-effect transistor

Devices. FET whose gate junction controls channel conduction.

JIC JTAG indirect configuration

FPGA. Altera programming-file type for indirect configuration-device programming.

JSON JavaScript object notation

Languages. Structured data format used for configurations, reports, and automation interfaces.

JTAG Joint Test Action Group

Test. Historical group name now commonly used for IEEE 1149.1 test access and related interfaces.

JTAG-to-AXI JTAG to AXI bridge

FPGA. Debug bridge allowing JTAG access to an AXI address space.

K**KGD** Known good die

Test. Die tested sufficiently for its intended integration and acceptance criteria.

KKT Karush-Kuhn-Tucker

Optimization. Constrained-optimization conditions for stationarity, feasibility, and complementarity under suitable assumptions; used in circuit-optimization analysis.

KL Kernighan-Lin

Optimization. Graph-partitioning heuristic exchanging vertices between balanced partitions to reduce cut cost; relevant to netlist partitioning.

KPI Key performance indicator

Core. Selected measure used to track design, flow, verification, or business performance.

L**L1** Level-one cache

Architecture. Cache level closest to the processor execution resources under the relevant hierarchy.

L2 Level-two cache

Architecture. Second cache level in a specified hierarchy.

L2S Liveness to safety

Formal. Transformation allowing certain liveness questions to be solved using safety-checking techniques.

L3 Level-three cache

Architecture. Third cache level in a specified hierarchy.

LAB Logic array block

FPGA. Altera FPGA grouping of logic resources.

L-BFGS Limited-memory BFGS

Optimization. Limited-memory quasi-Newton method for large smooth problems, including differentiable placement and parameter optimization.

L-BFGS-B Limited-memory BFGS with bounds

Optimization. Bound-constrained quasi-Newton method, applicable to differentiable circuit or placement parameter optimization with variable limits.

LBIST Logic built-in self-test

Test. Built-in testing of logic using generated patterns and compacted responses.

LC Logic cell

FPGA. FPGA capacity or resource term whose definition depends on the vendor.

LDD Lightly doped drain

Fabrication. Drain-extension structure intended to manage electric fields.

LDE Layout-dependent effect

Physical. Device behavior change caused by surrounding layout geometry and process interactions.

LDMOS Laterally diffused MOS

Devices. Lateral power MOS device commonly used in high-voltage and RF applications.

LDO Low-dropout regulator

Analog RF. Linear voltage regulator operating with a small input-to-output voltage difference.

LE Logic element

FPGA. Basic FPGA logic resource; exact composition is device-family-specific.

LEC Logical equivalence checking

Formal. Equivalence checking of logic representations, commonly before and after synthesis.

LEF Library exchange format

Languages. Abstract physical information about technology, routing layers, cells, and macros.

LELE Litho etch litho etch

Fabrication. Double-patterning sequence using two lithography and etch cycles.

LELELE Litho etch litho etch litho etch

Fabrication. Triple-patterning sequence using three lithography and etch cycles.

LER Line-edge roughness

Fabrication. Variation in the position of a patterned line edge.

LET Linear energy transfer

Reliability. Energy deposited per unit path length by an energetic particle.

LFM Latent fault metric

Reliability. Hardware architectural metric addressing latent multiple-point faults in ISO 26262.

LFSR Linear-feedback shift register

Test. Shift-register state machine using linear feedback, often for test patterns or signatures.

LGA Land grid array

Packaging. Package or connection arrangement using flat lands instead of protruding balls or pins.

LI Local interconnect

Physical. Short-range interconnect layer or structure near devices.

LIB Liberty library file

Languages. Common shorthand or extension for Liberty timing, power, and functional library data.

LIFO Last in first out

Architecture. Stack discipline or buffer returning the most recently added item first.

LIN Local interconnect network

Interfaces. Low-cost serial network commonly used for automotive peripheral functions.

LIVA Light-induced voltage alteration

Test. Failure-analysis technique observing voltage changes under optical excitation.

LLC Last-level cache

Architecture. Final shared or private cache level before the next memory hierarchy level.

LLM Large language model

AI/ML. Large neural language model used for RTL and EDA-script assistance, design documentation, and engineering question answering.

LLMOps Large language model operations
AI/ML. Operational practices for LLM-based applications and their evaluation.

LM Levenberg-Marquardt

Optimization. Damped nonlinear least-squares method used for fitting device or circuit-model parameters to measured or simulated responses.

LNA Low-noise amplifier

Analog RF. Amplifier designed to add little noise to a weak input signal.

LO Local oscillator

Analog RF. Oscillator signal used for frequency conversion in a receiver or transmitter.

LOC Launch on capture

Test. At-speed scan-test method launching a transition through a functional capture pulse.

LOCOS Local oxidation of silicon

Fabrication. Older field-isolation process using selective silicon oxidation.

LOD Length of diffusion

Physical. Layout dimension used in modeling stress-related device effects.

LoRA Low-rank adaptation

AI/ML. Fine-tuning method learning low-rank updates to selected model weights.

LOS Launch on shift

Test. At-speed scan-test method launching a transition using the final scan-shift operation.

LP Linear programming

Optimization. Optimization of a linear objective with linear constraints, used directly or as a relaxation of EDA design problems.

LP Low power

Power. Design methods or operating modes intended to reduce power consumption.

LPCVD Low-pressure chemical vapor deposition

Fabrication. CVD performed at reduced pressure.

LPDDR Low-power double-data-rate memory

Architecture. JEDEC DRAM family optimized for reduced power consumption.

LPE Layout parasitic extraction

Physical. Extraction of parasitic electrical elements from layout geometry.

LPF Low-pass filter

Analog RF. Filter passing lower frequencies while attenuating higher frequencies.

LRC Layout rule check

Physical. Generic layout-rule checking abbreviation; exact scope is tool-dependent.

LRDIMM Load-reduced dual in-line memory module

Architecture. DIMM using buffering to reduce electrical loading on the memory controller.

LRM Language reference manual

Languages. Authoritative description of a language's syntax and semantics.

LS Level shifter

Power. Circuit translating signals between voltage domains.

LSB Least significant bit

Analog RF. Lowest-weight digital bit or associated quantization step.

LSE Log-sum-exp

Optimization. Smooth approximation to a maximum, used in differentiable wirelength objectives for analytical placement.

LSF Load sharing facility

Ecosystem. IBM workload-management software used in compute farms, including EDA workloads.

LSI Large-scale integration

Core. Historical category of integrated-circuit complexity preceding VLSI.

LSQ Load-store queue

Architecture. Structure tracking in-flight memory operations and ordering dependencies.

LSSD Level-sensitive scan design

Test. Scan methodology using level-sensitive latches and controlled clocking.

LSTM Long short-term memory

AI/ML. Recurrent neural-network architecture with gated memory state.

LT Loosely timed

Verification. TLM modeling style emphasizing transaction-level timing with limited synchronization detail.

LTL Linear temporal logic

Formal. Temporal logic specifying properties along individual execution paths.

LTSSM Link training and status state machine

Interfaces. State machine controlling PCIe link initialization, training, and link-state transitions.

LU Lower-upper decomposition

AI/ML. Matrix factorization used to solve linear equation systems.

LUT Look-up table

Formal. Truth-table-based logic element or stored mapping used in implementation and modeling.

LVCMOS Low-voltage CMOS

Interfaces. CMOS I/O signaling family using lower supply voltages.

LVDS Low-voltage differential signaling

Interfaces. Differential signaling technology using small voltage swings.

LVF Liberty variation format

Timing. Liberty extensions for statistical variation data used in timing analysis.

LVP Laser voltage probing

Test. Optical probing of internal electrical activity using a laser.

LVPECL Low-voltage positive emitter-coupled logic

Interfaces. Lower-voltage PECL signaling family.

LVS Layout versus schematic

Physical. Checking that extracted layout connectivity matches a reference circuit or netlist.

LVT Low threshold voltage

Power. Device or cell option generally favoring speed over leakage.

LVTTTL Low-voltage transistor-transistor logic

Interfaces. Low-voltage I/O standard compatible with specified TTL-like thresholds.

LWR Line-width roughness

Fabrication. Variation in the width of a patterned line.

M**M1** Metal one

Physical. First designated metal routing layer; layer naming depends on the process.

MAC Media access control

Interfaces. Link-layer function managing medium access and frame-related operations.

MAC Multiply accumulate

Architecture. Arithmetic operation or datapath computing a product and adding it to an accumulator.

MAE Mean absolute error

AI/ML. Average absolute prediction error.

MAPE Mean absolute percentage error

AI/ML. Average absolute percentage error; problematic when target values approach zero.

MBE Molecular beam epitaxy

Fabrication. Epitaxial growth from molecular or atomic beams under high vacuum.

MBIST Memory built-in self-test

Test. Built-in execution of memory test algorithms.

MBU Multiple-bit upset

Reliability. One event causing errors in multiple stored bits.

MC Monte Carlo

Analog RF. Statistical simulation using random parameter samples to estimate variation and yield.

MCAD Mechanical computer-aided design

PCB SI. Mechanical modeling used alongside electronic design for enclosure and assembly integration.

MC/DC Modified condition and decision coverage

Verification. Coverage criterion checking that each condition can independently affect its decision outcome.

MCM Multi-chip module

Packaging. Package or module containing multiple integrated-circuit dies.

MCMM Multi-corner multi-mode

Timing. Alternative word order for multi-mode multi-corner analysis.

MCP Model context protocol

AI/ML. Protocol connecting AI applications to tools and context; distinct from multicycle path and multi-chip package.

MCP Multi-chip package

Packaging. Package containing multiple dies; distinct from multicycle path.

MCP Multicycle path

Timing. Timing path permitted more than the default clock-cycle relationship.

MCU Microcontroller unit

Architecture. Processor with integrated memory and peripherals for embedded control.

MCU Multiple-cell upset

Reliability. One event affecting multiple memory cells; distinct from microcontroller unit.

MDC Management data clock

Interfaces. Clock accompanying an Ethernet MDIO management interface.

MDIO Management data input and output

Interfaces. Management interface used to access Ethernet PHY registers.

MDP Markov decision process

AI/ML. Sequential-decision model with states, actions, transition probabilities, and rewards; distinct from mask data preparation.

MDP Mask data preparation

Fabrication. Preparation of layout data for mask writing and manufacturing.

MDV Metric-driven verification

Verification. Verification managed using explicit plans, metrics, and closure criteria.

MEB Multi-electron beam

Fabrication. Multiple-electron-beam patterning or mask-writing technology.

MEEF Mask-error enhancement factor

Fabrication. Sensitivity of wafer-level pattern error to mask-level dimensional error.

MEMS Microelectromechanical systems

Photonics. Microscale devices combining mechanical and electrical functions.

MESI Modified exclusive shared invalid

Architecture. Four-state cache-coherency protocol family.

MIG Majority-inverter graph

Formal. Logic graph based on majority operators and complemented edges.

MILP Mixed-integer linear programming

Optimization. Linear optimization combining integer and continuous variables, used for implementation choices and resource constraints.

MIMD Multiple instruction multiple data *Architecture*. Parallel execution model with independently controlled instruction streams.

MIP Mixed-integer programming *Optimization*. Optimization mixing integer and continuous variables for discrete and continuous design choices; often used specifically for MILP.

MIPI Mobile Industry Processor Interface *Interfaces*. Historical expansion of the MIPI Alliance name; current specifications use the MIPI brand.

MIQP Mixed-integer quadratic programming *Optimization*. Optimization with integer variables, a quadratic objective, and linear constraints; useful for quadratic-cost placement and allocation formulations.

MISR Multiple-input signature register *Test*. Linear compactor combining multiple response streams into a signature.

ML Machine learning *AI/ML*. Learning predictive or decision models from data, including timing, power, congestion, verification, and design-flow results.

MLAB Memory logic array block *FPGA*. Small embedded memory resource in selected Altera FPGA families.

MLIR Multi-level intermediate representation *Languages*. Compiler infrastructure supporting multiple abstraction levels and extensible intermediate representations.

MLOps Machine learning operations *AI/ML*. Practices for managing model training, deployment, monitoring, and reproducibility.

MLP Multilayer perceptron *AI/ML*. Feed-forward neural network built mainly from fully connected layers.

MM Machine model *Reliability*. Historical ESD test model; applicability depends on the qualification regime.

MMCM Mixed-mode clock manager *FPGA*. Clock-generation and conditioning resource in selected AMD/Xilinx devices.

MMI Multimode interference *Photonics*. Optical effect used for splitting, combining, and routing light.

MMIC Monolithic microwave integrated circuit *Analog RF*. Microwave circuit fabricated on a single semiconductor substrate.

MMIO Memory-mapped input and output *Architecture*. Access to device registers through the processor's memory-address space.

MMMC Multi-mode multi-corner *Timing*. Analysis across multiple functional modes and process, voltage, temperature, or RC corners.

MMP Minimum metal pitch *Physical*. Minimum center-to-center pitch for a specified metal layer or technology reference.

MMU Memory management unit *Architecture*. Hardware translating addresses and enforcing memory-access attributes or permissions.

MNA Modified nodal analysis *AI/ML*. Circuit-equation formulation augmenting node voltages with selected branch variables.

MOBO Multiobjective Bayesian optimization

Optimization. Bayesian optimization of competing circuit or flow objectives, seeking useful Pareto trade-offs with few expensive evaluations.

MOCVD Metal-organic chemical vapor deposition

Fabrication. CVD using metal-organic precursors, common in compound semiconductors.

MOEMS Micro-opto-electromechanical systems

Photonics. Microsystems combining optical, electrical, and mechanical functions.

MOESI Modified owned exclusive shared invalid

Architecture. Cache-coherency protocol family adding an owned state to MESI-like states.

MOL Middle of line

Core. Device-contact and local-interconnect processing between FEOL and BEOL.

MoM Method of moments

PCB SI. Numerical method commonly applied to integral-equation electromagnetic problems.

MOO Multiobjective optimization

Optimization. Optimization of competing objectives such as delay, power, area, yield, and simulation cost.

MOR Model order reduction

AI/ML. Reduction of a model's state dimension while retaining selected input-output behavior.

MOS Metal-oxide-semiconductor

Devices. Device structure underlying conventional MOS transistors and capacitors.

MOSFET Metal-oxide-semiconductor field-effect transistor

Devices. Insulated-gate transistor widely used in integrated circuits.

MPC Mask process correction

Fabrication. Mask-data correction for mask-manufacturing effects.

M-PHY MIPI M-PHY physical layer

Interfaces. MIPI physical-layer specification used by selected high-speed interfaces.

MPI Message passing interface

Ecosystem. Parallel-computing interface used for distributed numerical workloads.

MPNN Message-passing neural network

AI/ML. Graph-learning framework exchanging messages along edges; circuit models can encode cell, pin, net, or delay attributes.

MPU Memory protection unit

Architecture. Hardware checking memory access permissions without necessarily translating addresses.

MPU Microprocessor unit

Architecture. Processor device, often requiring more external system support than a microcontroller.

MPW Minimum pulse width

Timing. Minimum allowed duration of a clock or control pulse; distinct from multi-project wafer.

MPW Multi-project wafer

Core. Fabrication run sharing wafer and mask costs among multiple designs.

MRAM Magnetoresistive random-access memory

Architecture. Memory storing information through magnetic states and resistance differences.

MRC Mask rule checking

Fabrication. Checking mask patterns against mask-manufacturing constraints.

MRR Microring resonator

Photonics. Ring-shaped optical resonator used in filtering, modulation, and sensing.

MS Mixed signal

Analog RF. Combination of analog and digital functions in a circuit or model.

MSB Most significant bit

Analog RF. Highest-weight digital bit in a word.

MSCTS Multi-source clock tree synthesis

Physical. Clock distribution synthesis using multiple clock sources or roots for local trees.

MSE Mean squared error

AI/ML. Average squared prediction error.

MSHR Miss status holding register

Architecture. Structure tracking outstanding cache misses and associated requests.

MSI Medium-scale integration

Core. Historical integration category between small-scale and large-scale integration.

MSI Message-signaled interrupt

Interfaces. Interrupt delivered through a memory-write transaction; distinct from medium-scale integration.

MSI-X Extended message-signaled interrupts

Interfaces. PCI interrupt capability with a table-based vector organization.

MSL Moisture sensitivity level

Packaging. Classification guiding moisture handling and reflow exposure of packaged components.

MSR Model-specific register

Architecture. Processor control/status register with model-specific or architecture-defined behavior, commonly in x86 contexts.

MST Minimum spanning tree

Physical. Minimum-weight tree connecting all vertices without adding Steiner vertices.

MSV Multi-supply voltage

Power. Design methodology using multiple supply voltages.

MTBF Mean time between failures

Reliability. Expected interval between failures; used in synchronizer reliability and system dependability.

MTCMOS Multi-threshold CMOS

Power. Use of multiple threshold-voltage device types, often with power gating.

MTTF Mean time to failure

Reliability. Expected time until failure for a nonrepairable population or modeled failure mechanism.

MV Multi-voltage

Power. Design using more than one supply voltage.

MZI Mach-Zehnder interferometer

Photonics. Interferometer splitting and recombining optical paths to control interference.

MZM Mach-Zehnder modulator

Photonics. Optical modulator based on a Mach-Zehnder interferometer.

N

NA Numerical aperture

Fabrication. Optical measure governing resolution and depth-of-focus trade-offs.

NAG Nesterov accelerated gradient

Optimization. Gradient method using momentum or extrapolation, used in analytical global placement.

NAS Neural architecture search

AI/ML. Search over neural-network structures and associated design choices.

NBA Nonblocking assignment

Verification. SystemVerilog assignment form whose update is scheduled in the nonblocking-assignment region.

NBTI Negative bias temperature instability

Reliability. BTI associated with negative gate-bias stress, particularly in p-channel devices.

NCFET Negative-capacitance field-effect transistor

Devices. Device concept using negative-capacitance behavior to improve gate control.

NCG Nonlinear conjugate gradient

Optimization. Gradient-based optimization with conjugate-direction updates, used in nonlinear analytical placement and parameter optimization.

NCO Neural combinatorial optimization

AI/ML. Neural methods that construct or guide discrete solutions, relevant to placement, routing, and synthesis search.

NCO Numerically controlled oscillator

Analog RF. Digital generation of phase and waveform samples from numerical state.

N-detect Multiple-detection testing

Test. Test strategy targeting repeated detection of a modeled fault by distinct patterns.

NDM New data model

Languages. Synopsys library and design data model used in implementation flows.

NDR Nondefault routing rule

Physical. Routing rule overriding defaults, such as wider wires or larger spacing.

NEGF Nonequilibrium Green's function

Devices. Quantum-transport formalism used in advanced device simulation.

NEMS Nanoelectromechanical systems

Photonics. Electromechanical devices with nanoscale functional structures.

NEXT Near-end crosstalk

PCB SI. Coupled interference observed at the near end of a victim interconnect.

NF Noise figure

Analog RF. Noise degradation metric expressed relative to a specified reference temperature.

NILS Normalized image log slope

Fabrication. Dimensionless aerial-image contrast metric at an edge.

NIU Network interface unit

Interfaces. Block connecting an agent to a network or on-chip interconnect.

NLDM Nonlinear delay model

Timing. Table-based timing model, commonly indexed by input slew and output load.

NLM Nonlinear model

Timing. Generic modeling abbreviation; specify whether delay, power, or another quantity is meant.

NLP Natural language processing

AI/ML. Computation over human language, including EDA documentation and engineering requests.

NLP Nonlinear programming

Optimization. Optimization with nonlinear objectives or constraints, including device sizing and circuit-performance trade-offs; distinct from natural language processing.

NLPM Nonlinear power model

Timing. Table-based representation of cell power as a function of operating conditions.

NMOS N-channel MOS

Devices. MOS transistor or logic technology using electron-channel conduction.

NN Neural network

AI/ML. Parameterized computational model constructed from connected processing units.

NoC Network on chip

Interfaces. On-chip communication network connecting processing, memory, and peripheral blocks.

NPN N-type P-type N-type

Devices. Bipolar transistor structure with an n-type emitter and collector around a p-type base.

NPO Near-packaged optics

Photonics. Optical-engine placement close to a processor or switch package.

NPTH Nonplated through hole

PCB SI. Hole without conductive wall plating.

NPU Neural processing unit

Architecture. Processor or accelerator specialized for neural-network workloads.

NR Newton-Raphson

AI/ML. Iterative root-finding method used for nonlinear circuit equations.

NRE Nonrecurring engineering

Core. One-time development costs, including engineering effort and mask-related expenses.

NRZ Non-return-to-zero

PCB SI. Binary signaling in which the level does not return to a neutral value each bit.

NRZI Non-return-to-zero inverted

PCB SI. Encoding that conveys information through the presence or absence of transitions.

NSFET Nanosheet field-effect transistor

Devices. Transistor using nanosheet channels, commonly in a gate-all-around configuration.

NSGA-II Nondominated sorting genetic algorithm II

Optimization. Evolutionary multiobjective method using nondominated sorting and diversity preservation, applied to circuit-design trade-offs.

NVM Nonvolatile memory

Architecture. Memory retaining stored information without power.

NVMe Non-volatile memory express

Interfaces. Storage protocol designed for nonvolatile memory, commonly transported over PCIe.

NVP Number of violating paths

Timing. Count of failing timing paths under the report's enumeration settings.

NVRAM Nonvolatile random-access memory

Architecture. Random-access storage retaining data without normal operating power.

NWFET Nanowire field-effect transistor

Devices. Transistor using nanowire channels.

O

OA OpenAccess

Languages. EDA design database and API standard maintained by Si2.

OASIS Open Artwork System Interchange Standard

Languages. Compact layout exchange format defined by SEMI P39.

OASIS.MASK OASIS specific to mask tools

Languages. Mask-tool-oriented format defined by SEMI P44; associated with OASIS.

OBIRCH Optical beam induced resistance change

Test. Failure-localization technique measuring resistance changes caused by a scanned optical beam.

OC Operating condition

Timing. Library or analysis designation of process, voltage, and temperature settings.

OCC On-chip clock controller

Test. Controller generating or selecting clock pulses needed for at-speed testing.

OCD Optical critical dimension

Fabrication. Optical metrology inferring patterned structure dimensions from measured optical responses.

OCI Open compression interface

Test. Interface for describing on-chip scan compression, associated with IEEE 1450.6.1.

OCP Open Compute Project

Ecosystem. Organization supporting open computing infrastructure, including chiplet-related work.

OCP Open core protocol

Ecosystem. Core-interface protocol standardized through the OCP-IP and Accellera ecosystem.

OCV On-chip variation

Timing. Variation in device and interconnect behavior within a chip, modeled in timing analysis.

ODB++ ODB++ manufacturing data format

PCB SI. Electronic manufacturing-data exchange family. Retain the format name rather than relying on a historical expansion.

ODC Observability don't care

Formal. Condition under which a node's value cannot affect the observed outputs.

ODE Ordinary differential equation

AI/ML. Equation involving derivatives with respect to one independent variable.

ODM Original design manufacturer

Core. Supplier designing and manufacturing products for another company's branding.

ODSA Open domain-specific architecture

Ecosystem. Open Compute Project initiative associated with chiplets and domain-specific integration; related work now appears under Open Chiplet Economy.

ODT On-die termination

Architecture. Termination circuitry integrated into a device.

OEM Original equipment manufacturer

Core. Organization producing a finished product incorporating supplied components or subsystems.

OIO Optical input and output

Photonics. Optical communication interfaces associated with electronic systems or chips.

OIP3 Output third-order intercept point

Analog RF. Third-order intercept referred to the output.

ONNX Open neural network exchange

AI/ML. Interchange representation for trained machine-learning models.

OOC Out of context

FPGA. Synthesis or implementation of a block outside the full top-level design context.

OOD Out of distribution

AI/ML. Designs or conditions differing from training data, such as a new process node, circuit family, or implementation regime.

OOO Out of order

Architecture. Execution scheduling that issues ready operations outside original program order while preserving architectural rules.

OOP Object-oriented programming

Verification. Programming style supporting classes, inheritance, and polymorphism, used heavily in UVM.

OP Operating point

Analog RF. Steady circuit state used to initialize or linearize circuit analysis.

OPA Operational amplifier

Analog RF. Common abbreviation for a high-gain differential voltage amplifier; also a product-family prefix.

OPC Optical proximity correction

Fabrication. Modification of mask shapes to compensate for lithographic imaging distortions.

OPCG On-product clock generation

Test. Generation of test clocks on the device, often for at-speed scan test.

OpenDB Open database

Languages. OpenROAD's physical-design database; a project name rather than an industry-wide file standard.

OpenMP Open multi-processing

Ecosystem. Shared-memory parallel-programming interface used in engineering software.

OSAT Outsourced semiconductor assembly and test

Core. Provider of semiconductor packaging, assembly, and testing services.

OSFP Octal small form factor pluggable

Ecosystem. Pluggable transceiver module form factor relevant to optical system design.

OSNR Optical signal-to-noise ratio

Photonics. Optical signal power relative to noise power in a defined reference bandwidth.

OSPI Octal serial peripheral interface

Interfaces. SPI-derived interface using eight data lines in selected modes.

OSR Oversampling ratio

Analog RF. Sampling rate relative to the relevant Nyquist-rate signal bandwidth.

OSVVM Open source VHDL verification methodology

Verification. VHDL verification libraries and methodology supporting stimulus, coverage, checking, and automation.

OTA Operational transconductance amplifier

Analog RF. Amplifier producing output current proportional to differential input voltage.

OTP One-time programmable

Architecture. Memory or configuration element intended for one programming operation.

OVL Open verification library

Verification. Library of reusable assertion and checker components.

OVM Open verification methodology

Verification. Historical SystemVerilog verification methodology preceding UVM.

P

P1dB One-decibel compression point

Analog RF. Input or output power where gain compresses by one decibel.

PA Power amplifier

Analog RF. Amplifier delivering substantial output power to a load.

PAC Periodic AC analysis

Analog RF. Small-signal frequency analysis about a periodically varying operating point.

PAE Power-added efficiency

Analog RF. RF output power minus RF input power, divided by DC supply power.

PAL Programmable array logic

FPGA. Programmable logic architecture or historical product family with a programmable AND plane.

PAM Pulse amplitude modulation

PCB SI. Encoding information using pulse amplitude levels.

PAM4 Four-level pulse amplitude modulation

PCB SI. Signaling with four amplitude levels encoding two bits per symbol.

PASID Process address space identifier

Interfaces. Identifier associating device requests with a process address space.

PBA Path-based analysis

Timing. Timing recalculation along specific paths to reduce graph-based pessimism.

PBIST Programmable built-in self-test

Test. Built-in test engine whose algorithms or operating sequences can be programmed.

PBT Population-based training

AI/ML. Population search that adapts configurations during runs; supported in EDA flow autotuning frameworks.

PBTI Positive bias temperature instability

Reliability. BTI associated with positive gate-bias stress, particularly in n-channel devices.

PC Program counter

Architecture. Register identifying an instruction address in the architectural execution sequence.

PCA Principal component analysis

AI/ML. Linear dimensionality reduction using directions of maximum variance; distinct from printed circuit assembly.

PCA Printed circuit assembly

PCB SI. Alternative abbreviation for an assembled printed circuit board.

PCAP Processor configuration access port

FPGA. Processor-side configuration interface in selected AMD/Xilinx SoCs.

PCB Printed circuit board

PCB SI. Board carrying patterned conductive connections and mounted components.

PCBA Printed circuit board assembly

PCB SI. Board with installed components and completed assembly operations.

PCG Preconditioned conjugate gradient

AI/ML. Conjugate-gradient solution accelerated by a preconditioner.

PCI Peripheral component interconnect

Interfaces. Parallel computer expansion-bus standard preceding PCI Express.

PCIe Peripheral component interconnect express

Interfaces. High-speed serial interconnect architecture maintained by PCI-SIG.

PCI-SIG Peripheral Component Interconnect Special Interest Group

Interfaces. Organization maintaining PCI and PCI Express specifications.

PCM Phase-change memory

Architecture. Memory storing data through material phase-dependent resistance.

PCM Process control monitor

Fabrication. Test structures or measurements used to monitor semiconductor process behavior.

PCRAM Phase-change random-access memory

Architecture. Alternative abbreviation emphasizing random access in phase-change memory.

PCS Physical coding sublayer

Interfaces. Physical-layer sublayer handling encoding, alignment, and related symbol processing.

PD Photodetector

Photonics. Device converting incident light into an electrical response.

PD Physical design

Physical. Transformation of logical design into placed and routed physical structures.

PD Power delivery

Interfaces. USB power-negotiation specification context; distinct from physical design and power domain.

PD Power domain

Power. Set of design elements sharing a specified power-supply intent.

PDE Partial differential equation

AI/ML. Equation involving derivatives with respect to multiple independent variables.

PDF Path delay fault

Test. Fault model representing excessive delay along a specified path.

PKD Process design kit

Core. Foundry-specific models, rules, layers, and supporting data needed to design for a process.

PDL Procedural description language

Test. IEEE 1687 language describing operations on embedded instruments.

PDN Power delivery network

Physical. Network supplying electrical power from its source to circuit loads.

PDP Power-delay product

Power. Combined power and delay metric; interpretation depends on the measured operation.

PDR Property-directed reachability

Formal. Safety-verification method closely related to IC3.

PD-SOI Partially depleted silicon on insulator

Devices. SOI technology in which part of the transistor body remains undepleted.

PECL Positive emitter-coupled logic

Interfaces. Emitter-coupled logic operated with a positive supply arrangement.

PECVD Plasma-enhanced chemical vapor deposition

Fabrication. CVD using plasma activation to enable or accelerate reactions.

PEEC Partial element equivalent circuit

PCB SI. Electromagnetic modeling method representing structures with circuit-equivalent partial elements.

PEFT Parameter-efficient fine-tuning

AI/ML. Adaptation updating a limited set of parameters or added modules.

PER Packet error ratio

PCB SI. Fraction of packets received with errors or declared unsuccessful under stated rules.

PERC Programmable electrical rule checking

Physical. Programmable reliability and electrical checks; also part of Siemens Calibre naming.

PEX Parasitic extraction

Physical. Derivation of parasitic resistance, capacitance, and potentially inductance from physical structures.

PF Physical function

Interfaces. Fully featured PCIe function managing associated virtualization resources.

PFA Physical failure analysis

Test. Physical investigation of defects using imaging, sectioning, and related methods.

PFD Phase-frequency detector

Analog RF. Circuit detecting phase and frequency differences for a control loop.

PFM Pulse-frequency modulation

Analog RF. Control by varying pulse repetition frequency.

PG Power and ground

Physical. Supply connections, nets, or routing structures.

PG Power gating

Power. Disconnection of a circuit region from its supply to reduce leakage.

PGA Pin grid array

Packaging. Package with a grid of pins; distinct from programmable-gain amplifier.

PGA Programmable-gain amplifier

Analog RF. Amplifier whose gain is selected digitally or through discrete settings.

PGN Power and ground network

Physical. Supply-distribution network; often used interchangeably with PDN in physical design.

pHEMT Pseudomorphic high-electron-mobility transistor

Devices. HEMT using a strained pseudomorphic layer structure.

PHY Physical layer

Interfaces. Circuit and protocol functions implementing physical signaling and link attachment.

PI Power integrity

PCB SI. Adequacy and stability of power delivery to circuit loads.

PIC Photonic integrated circuit

Photonics. Integrated circuit manipulating light through on-chip optical components.

PIH Pin in hole

PCB SI. Through-hole insertion or reflow process terminology.

PIM Processing in memory

Architecture. Processing placed within memory devices or their closely coupled structures.

PIN P-type intrinsic N-type

Photonics. Semiconductor diode structure widely used for photodetection and other functions.

PiP Package in package

Packaging. Integration of a packaged component within another package.

PIPE PHY interface for PCI Express and other architectures

Interfaces. Interface between controller logic and a PHY; official scope and expansion vary by specification revision.

PJ Periodic jitter

PCB SI. Timing modulation with periodic components.

PL Programmable logic

FPGA. Reconfigurable hardware fabric, often contrasted with a hard processor subsystem.

PLA Programmable logic array

FPGA. Logic architecture with programmable AND and OR planes.

PLD Programmable logic device

FPGA. General category of devices whose logic function is programmed after manufacture.

PLI Programming language interface

Languages. Verilog interfaces allowing external code to access or extend simulation.

PLL Phase-locked loop

Analog RF. Feedback system aligning an oscillator's phase with a reference relationship.

PM Phase margin

Analog RF. Phase separation from instability at the selected unity loop-gain crossing.

PMA Physical medium attachment

Interfaces. Sublayer handling functions such as serialization and clock recovery.

PMD Physical medium dependent

Interfaces. Portion of a physical-layer specification dependent on the transmission medium.

PMHF Probabilistic metric for random hardware failures

Reliability. ISO 26262 quantitative assessment of safety-goal violation due to random hardware failures.

PMIC Power management integrated circuit

Power. Chip providing regulated supplies and related power-management functions.

PMOS P-channel MOS

Devices. MOS transistor or logic technology using hole-channel conduction.

PMU Power management unit

Power. Controller coordinating power states, voltage levels, clocks, and power sequencing.

PNoise Periodic noise analysis

Analog RF. Noise analysis about a periodic steady-state solution; simulator spelling varies.

PNP P-type N-type P-type

Devices. Bipolar transistor structure complementary to NPN.

PnR Place and route

Physical. Alternative spelling of P&R.

POCV Parametric on-chip variation

Timing. Statistical variation treatment using parametric delay variation models.

POD Proper orthogonal decomposition

AI/ML. Model-reduction method based on dominant modes of data or system responses.

POF Programmer object file

FPGA. Altera programming data format for supported programmable devices.

POMDP Partially observable Markov decision process

AI/ML. Decision model in which the agent does not directly observe the full state.

PoP Package on package

Packaging. Stacked packaging arrangement joining packaged components.

POS Product of sums

Formal. Two-level Boolean expression formed by AND-ing sum terms.

POST Power-on self-test

Test. Self-test performed when a device or system powers up.

PPA Power performance and area

Core. Principal implementation objectives, often traded against one another during optimization.

PPAC Power performance area and cost

Core. PPA extended with manufacturing or product cost considerations.

PPO Proximal policy optimization

AI/ML. Policy-gradient reinforcement-learning algorithm using controlled policy updates; used in circuit-placement learning frameworks.

P&R Place and route

Physical. Placement of design instances and routing of their electrical connections.

PR Partial reconfiguration

FPGA. Reconfiguration of part of a programmable device while preserving other configured regions.

PR Precision-recall

AI/ML. Classifier evaluation relating precision to recall as a threshold changes; useful with rare hotspots or defects.

PRBS Pseudorandom binary sequence

PCB SI. Deterministic binary test sequence used to exercise links and measure performance.

PRI Page request interface

Interfaces. PCIe mechanism for requesting resolution of missing address translations or pages.

PRIMA Passive reduced-order interconnect macromodeling algorithm

AI/ML. Model-reduction method for passive interconnect macromodels.

PRNG Pseudorandom number generator
Reliability. Deterministic algorithm producing an apparently random sequence from an internal state.

PROM Programmable read-only memory
Architecture. Memory programmed after manufacturing, often only once.

PRPG Pseudorandom pattern generator
Test. Circuit generating pseudorandom test stimuli.

PS Processing system
FPGA. Hard processor subsystem in selected AMD/Xilinx adaptive SoCs.

PSL Property specification language
Verification. Assertion language standardized by IEEE 1850.

PSM Phase-shift mask
Fabrication. Mask using phase differences to modify interference and improve imaging.

PSM Pulse-skipping mode
Analog RF. Light-load control that omits selected switching pulses.

PSO Particle swarm optimization
Optimization. Population search using personal and collective search history, applied to analog parameter and design-space optimization.

PSP Penn State Philips
Devices. Surface-potential-based compact MOS model combining developments originating at Penn State and Philips.

PSRR Power-supply rejection ratio
Analog RF. Measure of sensitivity to supply perturbations; input- and output-referred conventions differ.

PSS Periodic steady state
Analog RF. Steady-state circuit analysis for periodically driven systems; distinct from portable stimulus.

PSS Portable test and stimulus standard
Verification. Accellera standard for reusable scenario descriptions; commonly called Portable Stimulus Standard.

PST Power state table
Power. Power-intent description of permitted combinations of supply or domain states.

PSTB Periodic stability analysis
Analog RF. Stability analysis around a periodic operating state.

PT PrimeTime
Ecosystem. Synopsys timing-analysis product shorthand.

PTAT Proportional to absolute temperature
Analog RF. Quantity designed to vary approximately with absolute temperature.

PTE Page table entry
Architecture. Record describing an address translation and its attributes.

PTH Plated through hole
PCB SI. Hole with conductive plating joining relevant board layers.

PTW Page table walker
Architecture. Hardware or mechanism reading page tables to resolve address translations.

PUF Physically unclonable function
Reliability. Circuit exploiting manufacturing variation to derive device-specific responses.

PVB Process variation band
Fabrication. Envelope of pattern contours across process conditions.

PVD Physical vapor deposition

Fabrication. Film deposition by physical vapor transport, including sputtering and evaporation.

PVT Process voltage and temperature

Timing. Operating and manufacturing conditions used to characterize circuit behavior.

PVTA Process voltage temperature and aging

Timing. PVT extended to include aging-dependent behavior.

PW Process window

Fabrication. Range of process settings yielding acceptable pattern or device results.

PWB Printed wiring board

PCB SI. Alternative term emphasizing the unpopulated board and its wiring.

PWM Pulse-width modulation

Analog RF. Control by varying pulse width or duty cycle.

PX PrimeTime PX

Ecosystem. Historical Synopsys power-analysis product shorthand, retained in legacy flows; the current power-analysis offering is PrimePower. PX alone has no universal expansion.

PXF Periodic transfer function

Analog RF. Transfer-function analysis around a periodically varying operating point.

PZ Pole-zero analysis

Analog RF. Computation of poles and zeros of a linearized circuit response.

Q

Q Quality factor

Analog RF. Dimensionless measure of resonator energy storage relative to energy loss.

Q3D Q3D Extractor

Ecosystem. Ansys parasitic-extraction product name; no generic acronym expansion is assigned.

QBF Quantified Boolean formula

Formal. Boolean formula containing existential or universal variable quantification.

QFN Quad flat no-lead

Packaging. Leadless package with contacts arranged around its perimeter.

QFP Quad flat package

Packaging. Package with leads extending from four sides.

QM Quality management

Reliability. ISO 26262 classification indicating ordinary quality management rather than an ASIL assignment.

QoR Quality of results

Core. Quality of an implementation measured by selected objectives and constraint satisfaction.

QoS Quality of service

Interfaces. Mechanisms controlling latency, bandwidth, priority, or fairness among competing traffic classes.

QP Quadratic programming

Optimization. Optimization of a quadratic objective with linear constraints, used in quadratic placement and local optimization subproblems.

QPF Quartus project file

Languages. Quartus project-level metadata file.

QPNOISE Quasiperiodic noise analysis

Analog RF. Noise analysis around a quasiperiodic operating solution.

QPSS Quasiperiodic steady state

Analog RF. Analysis of nonlinear circuits driven by multiple generally incommensurate fundamental frequencies.

QSF Quartus settings file

Languages. Quartus project-assignment and configuration file.

QSFP Quad small form factor pluggable

Ecosystem. Pluggable transceiver module family.

QSPI Quad serial peripheral interface

Interfaces. SPI-derived interface transferring data on four data lines in selected modes.

QTM Quick timing model

Timing. Simplified timing model created from timing constraints or high-level block information.

R

R2R Run-to-run control

Fabrication. Adjustment of process settings between runs based on prior measurements.

RAG Retrieval-augmented generation

AI/ML. Generation conditioned on retrieved information, such as EDA manuals, design documents, and engineering records.

RAL Register abstraction layer

Verification. Verification representation of addressable registers and their access behavior.

RAM Random-access memory

Architecture. Memory permitting access to addressed locations without sequential traversal.

RAS Reliability availability and serviceability

Architecture. System features supporting dependable operation, recovery, and maintenance.

RBB Reverse body bias

Power. Body bias that generally increases threshold magnitude to reduce leakage.

RBF Raw binary file

FPGA. Raw configuration-data format in selected FPGA flows; generic elsewhere.

RBT Raw bit file

FPGA. Textual raw-bitstream representation in selected FPGA tool flows.

RC Resistance and capacitance

Timing. Interconnect parameters determining loading, delay, and aspects of signal behavior.

RCD Registering clock driver

Architecture. DDR memory-module device registering commands and distributing clock-related signals.

RCmax Maximum RC corner

Timing. Corner name for a high-parasitic interconnect condition; exact construction is process-specific.

RCmin Minimum RC corner

Timing. Corner name for a low-parasitic interconnect condition; exact construction is process-specific.

RCWA Rigorous coupled-wave analysis

Photonics. Frequency-domain method for periodic optical structures.

RCX Resistance and capacitance extraction

Physical. Extraction of interconnect resistance and capacitance.

RDC Reset-domain crossing

Verification. Signal interaction across independently controlled reset domains.

RDIMM Registered dual in-line memory module

Architecture. DIMM using registered command/address signaling.

RDL Redistribution layer

Packaging. Interconnect layer relocating die connections to a desired pitch or location.

ReRAM Resistive random-access memory *Architecture*. Memory storing data through programmable resistance states.

REST Representational state transfer *Ecosystem*. Architectural style often used for web-accessible automation services.

RET Resolution enhancement technology *Fabrication*. Lithography methods improving printable resolution or process margin; distinct from state retention.

RET Retention *Power*. Preservation of selected state while a power domain is otherwise shut down.

RF Radio frequency *Analog RF*. Frequency range and circuit techniques used for radio communication and related applications.

RF Random forest *AI/ML*. Ensemble of decision trees; distinguish register file and radio frequency.

RF Register file *Architecture*. Bank of registers accessed by a processor datapath; distinct from radio frequency.

RFF Retention flip-flop *Power*. Flip-flop with retained state across specified power-down conditions.

RFFE Radio-frequency front end *Interfaces*. RF circuitry near antenna interfaces; also names a MIPI control-interface specification.

RFIC Radio-frequency integrated circuit *Analog RF*. Integrated circuit implementing radio-frequency functions.

RGMII Reduced gigabit media-independent interface *Interfaces*. Reduced-pin interface between an Ethernet MAC and PHY.

RHBD Radiation hardening by design *Reliability*. Circuit and layout techniques improving radiation tolerance.

RHBP Radiation hardening by process *Reliability*. Process modifications intended to improve radiation tolerance.

RIE Reactive ion etching *Fabrication*. Plasma etching combining chemical reaction and ion bombardment.

RISC Reduced instruction set computer *Architecture*. Processor-design approach favoring a comparatively regular instruction set and implementation model.

RISC-V Reduced instruction set computer five *Architecture*. Open instruction-set architecture family; V denotes the fifth Berkeley RISC design lineage.

RJ Random jitter *PCB SI*. Stochastic timing variation, often modeled with a Gaussian component.

RL Reinforcement learning *AI/ML*. Learning design decisions from rewards, including macro placement, synthesis choices, and circuit sizing.

RL Return loss *PCB SI*. Measure of reflected signal magnitude relative to the incident signal.

RLC Resistance inductance and capacitance *Timing*. Interconnect model including inductive effects as well as resistance and capacitance.

RLGC Resistance inductance conductance and capacitance *PCB SI*. Distributed transmission-line parameters including conductor and dielectric loss.

RLHF Reinforcement learning from human feedback

AI/ML. Model-training approach using human feedback to shape a learned reward or policy.

RMG Replacement metal gate

Fabrication. Process in which a temporary gate is replaced by the final metal gate stack.

RMS Root mean square

PCB SI. Quadratic-average measure used for noise, jitter, current, and voltage.

RMSE Root mean squared error

AI/ML. Square root of MSE, expressed in the target quantity's units.

RMST Rectilinear minimum spanning tree

Physical. Spanning tree using rectilinear distance as its edge metric.

RMW Read modify write

Architecture. Operation sequence reading data, modifying selected content, and writing the result.

RNM Real-number modeling

Analog RF. Modeling analog quantities with real-valued signals in an event-driven simulator.

RNN Recurrent neural network

AI/ML. Network using recurrent state to process sequences or iterative dynamics.

ROB Reorder buffer

Architecture. Structure tracking in-flight instructions and enabling ordered retirement.

ROBDD Reduced ordered binary decision diagram

Formal. Canonical BDD for a fixed variable order after reduction rules are applied.

ROC Receiver operating characteristic

AI/ML. Curve of true-positive against false-positive rate across thresholds, used to assess EDA classifiers.

ROM Read-only memory

Architecture. Nonvolatile memory intended primarily for reading after programming or manufacture.

ROM Reduced-order model

AI/ML. Lower-dimensional approximation of a larger model; distinct from read-only memory.

RoT Root of trust

Reliability. Trusted foundation supporting security functions such as authentication or secure boot.

RPC Remote procedure call

Ecosystem. Mechanism invoking a procedure in another process or machine.

RRAM Resistive random-access memory

Architecture. Alternative abbreviation for ReRAM.

RSMT Rectilinear Steiner minimum tree

Physical. Minimum-length rectilinear connection tree allowing additional Steiner points.

RSPF Reduced standard parasitic format

Languages. Reduced parasitic representation intended to simplify circuit loading and delay analysis.

RTA Rapid thermal annealing

Fabrication. Short high-temperature annealing step with rapid heating and cooling.

Rth Thermal resistance

Power. Temperature rise per unit heat flow under a specified thermal path.

RTL Register-transfer level

Core. Design abstraction describing registers and the combinational transformations between them.

RT-level Register-transfer level

Core. Alternative abbreviation for the RTL abstraction; see RTL.

RTLIL RTL intermediate language
Languages. Yosys internal representation and associated textual format.

RTL-to-GDSII Register-transfer level to GDSII

Core. Flow shorthand for digital synthesis and physical implementation through layout delivery.

RTN Random telegraph noise

Devices. Discrete stochastic fluctuations caused by trapping and detrapping processes.

RTP Rapid thermal processing

Fabrication. Broader family of rapid thermal wafer-processing operations.

RTS Random telegraph signal

Devices. Time-domain signal with discrete random switching between levels.

RUDY Rectangular uniform wire density

Physical. Fast placement-based routing-demand estimate.

RVE Results viewing environment

Physical. Calibre environment for inspecting verification results.

RVT Regular threshold voltage

Power. Nominal threshold-voltage device or cell option; compare SVT conventions.

S

SA Simulated annealing

Optimization. Stochastic search accepting some worsening moves under a temperature schedule, used in floorplanning, placement, and partitioning.

SA0 Stuck at zero

Test. Fault model forcing a signal to logic zero.

SA1 Stuck at one

Test. Fault model forcing a signal to logic one.

SaaS Software as a service

Ecosystem. Software delivered as a hosted service, including some cloud EDA offerings.

SAB Silicide block

Fabrication. Layer or process feature preventing silicide formation in selected regions.

SAC Self-aligned contact

Fabrication. Contact formation aligned to existing structures to improve process tolerance.

SAC Soft actor-critic

AI/ML. Entropy-regularized actor-critic algorithm; distinct from self-aligned contact.

SADP Self-aligned double patterning

Fabrication. Spacer-based pattern multiplication producing doubled pattern density.

SA-EDI Security annotation for electronic design integration

Languages. Accellera specification for communicating security-relevant properties of hardware IP.

SAF Stuck-at fault

Test. Fault model in which a signal remains at a constant logic value.

SAIF Switching activity interchange format

Languages. Activity statistics used for power estimation and optimization.

SAM Scanning acoustic microscopy

Packaging. Acoustic imaging used to detect package voids, cracks, and delamination.

SAQP Self-aligned quadruple patterning

Fabrication. Self-aligned pattern multiplication producing approximately quadrupled density.

SAR Successive approximation register
Analog RF. Register and conversion architecture used in successive-approximation ADCs.

SAS Serial attached SCSI
Interfaces. Serial enterprise-storage interface using the SCSI command model.

SAT Boolean satisfiability
Formal. Problem of determining whether a Boolean formula has a satisfying assignment.

SATA Serial ATA
Interfaces. Serial storage interface derived from the ATA command ecosystem.

SAW Surface acoustic wave
Photonics. Acoustic-wave technology using waves near a material surface.

SBO Surrogate-based optimization
Optimization. Search guided by a cheaper model of simulation or implementation results, reducing expensive EDA evaluations.

SC Switched capacitor
Analog RF. Circuit technique using clocked capacitors to implement charge transfer and effective impedances.

SCA Side-channel analysis
Reliability. Analysis of unintended leakage such as power, timing, or electromagnetic emissions.

SCC Strongly connected component
Formal. Maximal directed-graph region whose vertices are mutually reachable.

SCE Short-channel effects
Devices. Device behavior changes as channel length becomes comparable to electrostatic characteristic lengths.

SCE-MI Standard co-emulation modeling interface
Verification. Standard interface connecting software models with hardware emulation environments.

SCOAP Sandia controllability and observability analysis program
Test. Structural testability measures estimating signal controllability and observability.

SCSI Small computer system interface
Interfaces. Storage and peripheral command/interface architecture.

S/D Source and drain
Fabrication. Transistor terminal regions formed during device fabrication.

SD Secure Digital
Interfaces. Memory-card and interface standard name.

SDC Satisfiability don't care
Formal. Input combination impossible because of upstream logic; distinct from Synopsys Design Constraints.

SDC Synopsys design constraints
Languages. Tcl-based constraint format describing clocks, timing exceptions, and related design constraints.

SDD Small delay defect
Test. Delay defect potentially too small for conventional transition testing to detect reliably.

SDF Standard delay format
Languages. Exchange format for timing delays and timing checks, commonly used for back-annotation.

SDF Synchronous dataflow
Verification. Computation model with fixed token production and consumption rates; distinct from Standard Delay Format.

SDIO Secure Digital input and output

Interfaces. Extension of the SD interface for peripheral I/O functions.

SDM Sigma-delta modulator

Analog RF. Oversampling noise-shaping modulator used in conversion and frequency synthesis.

SDP Semidefinite programming

Optimization. Optimization with positive-semidefinite matrix constraints, used in convex design formulations and relaxations of difficult EDA problems.

SDRAM Synchronous dynamic random-access memory

Architecture. DRAM with an interface synchronized to a clock.

SEB Single-event burnout

Reliability. Destructive single-event failure involving excessive localized current or energy.

SEC Sequential equivalence checking

Formal. Equivalence checking that accounts for state evolution across clock cycles.

SECCDED Single-error correction double-error detection

Reliability. Code capability correcting one bit error and detecting two-bit errors within its codeword assumptions.

SEE Single-event effect

Reliability. Device response caused by an individual energetic particle interaction.

SEFI Single-event functional interrupt

Reliability. Single-event-induced disruption of a device's intended functionality.

SEGR Single-event gate rupture

Reliability. Destructive gate-dielectric damage caused by a single energetic particle event.

SEL Single-event latchup

Reliability. Particle-induced latchup that can require power removal and may cause damage.

SEM Scanning electron microscopy

Fabrication. Electron-beam imaging used for inspection, dimensions, and failure analysis.

SEMI Semiconductor Equipment and Materials International

Ecosystem. Historical expansion of the SEMI industry-association name.

SER Soft error rate

Reliability. Rate of transient state errors, often induced by radiation.

SerDes Serializer deserializer

Interfaces. Circuit converting between parallel data and serial signaling.

SET Single-event transient

Reliability. Transient pulse caused by a single energetic particle interaction.

SEU Single-event upset

Reliability. Radiation-induced change of stored state without necessarily causing permanent damage.

SF Slow-fast process corner

Timing. Mixed transistor corner complementary to FS under the same foundry convention.

SFDR Spurious-free dynamic range

Analog RF. Separation between the desired signal and the largest spur under stated conditions.

SFT Supervised fine-tuning

AI/ML. Model adaptation using labeled input-output examples, such as domain-specific EDA questions and verified scripts.

SGD Stochastic gradient descent

AI/ML. Gradient-based optimization using sampled data or minibatches.

SGMII Serial gigabit media-independent interface

Interfaces. Serial MAC-to-PHY interface for gigabit Ethernet contexts.

S/H Sample and hold

Analog RF. Circuit that samples an input and holds its value for subsequent processing.

SHA Sample-and-hold amplifier

Analog RF. Amplified sample-and-hold circuit.

SI International System of Units

Ecosystem. International measurement-unit system; SI derives from the French name *Système international d'unités*. Distinguish signal integrity.

SI Signal integrity

PCB SI. Preservation of intended signal quality across interconnects and circuit interfaces.

Si2 Silicon Integration Initiative

Ecosystem. Organization developing EDA interoperability and design infrastructure standards.

SIB Segment insertion bit

Test. IEEE 1687 network element controlling inclusion of a scan segment.

SiC Silicon carbide

Devices. Wide-bandgap semiconductor used particularly in high-voltage power devices.

SiGe Silicon germanium

Devices. Semiconductor alloy used in strained devices and heterojunction bipolar processes.

SIL Safety integrity level

Reliability. Integrity classification used in functional-safety standards such as IEC 61508.

SIMD Single instruction multiple data

Architecture. Execution model applying one instruction to multiple data elements.

SIMS Secondary ion mass spectrometry

Fabrication. Composition analysis based on sputtered secondary ions.

SIMT Single instruction multiple threads

Architecture. Execution model grouping threads under shared instruction issue with per-thread state.

SINAD Signal-to-noise and distortion ratio

Analog RF. Common converter and receiver metric including noise and distortion in the denominator.

SIP Semiconductor intellectual property

Core. Reusable semiconductor design assets; distinguish SiP, system in package.

SiP System in package

Packaging. Multiple functions or dies integrated within a common package.

SiPh Silicon photonics

Photonics. Photonic-device and circuit technology based on silicon-compatible manufacturing.

SIR Static IR drop

Physical. Supply drop computed from a static or averaged current model.

SIS SIS logic synthesis system

Formal. Historical Berkeley environment for sequential and combinational logic synthesis; the primary report uses SIS as a system name without a letter-by-letter expansion.

SISR Single-input signature register

Test. Signature register compacting a single serial response stream.

SKILL SKILL

Languages. Cadence extension language name; no generic expansion is assigned here.

SL Supervised learning

AI/ML. Learning from labeled examples, such as netlists paired with measured timing, power, or congestion results.

Slew Signal transition time

Timing. Common timing term for the time between specified voltage thresholds; not an acronym.

SLIMbus Serial low-power inter-chip media bus

Interfaces. MIPI interface for carrying digital audio and control between components.

SLM Silicon lifecycle management

Test. Monitoring, analysis, and optimization of silicon behavior across design, production, and operation.

SLM Small language model

AI/ML. Relative label for a smaller language model; distinct from silicon lifecycle management.

SLT System-level test

Test. Testing in a system or system-like environment using realistic workloads and interactions.

SLVT Super-low threshold voltage

Power. Foundry-specific low-threshold device or cell designation.

SMBO Sequential model-based optimization

Optimization. Iterative fitting of a performance model and selection of new evaluations; used in EDA flow and parameter tuning.

SMD Surface-mount device

PCB SI. Component designed for surface mounting.

SMMU System memory management unit

Architecture. Arm system-level address-translation and protection architecture.

SMO Source-mask optimization

Fabrication. Joint optimization of illumination source and mask pattern.

SMPS Switched-mode power supply

Analog RF. Power converter using switching devices and energy-storage components.

SMT Satisfiability modulo theories

Formal. Satisfiability solving with theories such as bit vectors, arrays, or arithmetic.

SMT Surface-mount technology

PCB SI. Assembly method mounting components on the board surface; distinct from satisfiability modulo theories.

SNDR Signal-to-noise-and-distortion ratio

Analog RF. Ratio of signal power to combined noise and distortion power.

SNR Signal-to-noise ratio

Analog RF. Ratio of desired signal power to noise power over a defined bandwidth.

SOA Safe operating area

Reliability. Operating region in which a device meets defined electrical and thermal limits.

SOA Semiconductor optical amplifier

Photonics. Semiconductor device amplifying optical signals; distinct from safe operating area.

SoC System on chip

Core. Integration of processors, interconnect, memory interfaces, and other functions on one chip.

SOCp Second-order cone programming

Optimization. Convex optimization with second-order cone constraints, applicable to suitable circuit-design and robust-design formulations.

SOcV Statistical on-chip variation

Timing. Statistical variation methodology; exact modeling details depend on the timing tool.

SODIMM Small-outline dual in-line memory module

Architecture. Compact DIMM form factor.

SOF SRAM object file

FPGA. Altera file containing SRAM-based FPGA configuration data.

SOI Silicon on insulator

Devices. Technology with an active silicon layer over an insulating layer.

SOIC Small-outline integrated circuit

Packaging. Package family; distinguish mixed-case SoIC, TSMC's system-on-integrated-chips technology.

SoIC System on integrated chips

Packaging. TSMC three-dimensional integration technology family.

SOP Sum of products

Formal. Two-level Boolean expression formed by OR-ing product terms.

SOT Start of test

Test. Event or timestamp marking commencement of a test operation.

SOT-MRAM Spin-orbit torque MRAM

Architecture. MRAM switching magnetic states using spin-orbit torque.

SoW System on wafer

Packaging. Wafer-scale system integration; also used in vendor technology names.

SP Stack pointer

Architecture. Register identifying the current stack location under a calling convention.

SPAD Single-photon avalanche diode

Photonics. Avalanche photodiode operated to detect individual photon events.

S-parameter Scattering parameter

PCB SI. Frequency-domain representation relating incident and reflected waves at network ports.

SPC Statistical process control

Fabrication. Statistical monitoring of a process to detect shifts and abnormal variation.

SPD Serial presence detect

Architecture. Memory-module information storage and access mechanism used for configuration.

SPEF Standard parasitic exchange format

Languages. Exchange format for interconnect parasitic resistance, capacitance, and related connectivity.

SPF Standard parasitic format

Languages. Parasitic-description format family; distinguish SPEF, which is a different format.

SPFM Single-point fault metric

Reliability. Hardware architectural metric addressing single-point and residual faults in ISO 26262.

SPI Serial peripheral interface

Interfaces. Synchronous serial peripheral connection using clock and selected data/control signals.

SPICE Simulation program with integrated circuit emphasis

Analog RF. Circuit-simulation program family and widely used netlist and modeling conventions.

SpMM Sparse matrix-matrix multiplication

AI/ML. Matrix multiplication involving sparse operands.

SpMV Sparse matrix-vector multiplication

AI/ML. Operation central to many sparse numerical and graph computations.

SQP Sequential quadratic programming

Optimization. Nonlinear optimization through quadratic subproblems, applicable to circuit sizing with smooth objectives and constraints.

SR Slew rate

Analog RF. Maximum large-signal rate of output-voltage change under stated conditions.

SRAF Subresolution assist feature

Fabrication. Mask feature improving imaging of nearby patterns without intentionally printing itself.

SRAM Static random-access memory

Architecture. Memory retaining state while powered without periodic refresh.

SRH Shockley-Read-Hall

Devices. Trap-assisted generation and recombination model.

SR-IOV Single-root I/O virtualization

Interfaces. PCIe capability allowing a physical function to expose multiple virtual functions.

SRL Shift register LUT

FPGA. Lookup-table resource configured as a shift register in supported FPGA architectures.

SRPG State-retention power gating

Power. Power gating that preserves selected state for later restoration.

SS Slow-slow process corner

Timing. Corner with slow NMOS and slow PMOS behavior in a specified process convention.

SS Subthreshold swing

Devices. Gate-voltage change required for a decade change in subthreshold drain current.

SSI Small-scale integration

Core. Historical category for integrated circuits containing relatively few logic functions.

SSL Self-supervised learning

AI/ML. Learning from targets derived from circuit data itself, for example masked or related graph representations.

SSL Semi-supervised learning

AI/ML. Learning from both labeled and unlabeled designs when simulation or implementation labels are expensive.

SSN Simultaneous switching noise

PCB SI. Noise caused by multiple outputs or circuits switching together; distinct from streaming scan network.

SSN Streaming scan network

Test. Siemens Tessent packetized scan-test delivery architecture.

SSO Simultaneous switching outputs

PCB SI. Outputs transitioning together, generating shared supply and return-path disturbances.

SSTA Statistical static timing analysis

Timing. Timing analysis representing delay variation statistically rather than using only fixed corners.

SSTL Stub series terminated logic

Interfaces. I/O signaling standard family commonly used with memory interfaces.

STA Static timing analysis

Timing. Analysis of timing paths and constraints without enumerating functional simulation stimulus.

STB Stability analysis

Analog RF. Loop stability analysis, often using a probe-based small-signal method.

STCO System technology co-optimization

Core. Joint optimization across system architecture, integration, packaging, and semiconductor technology.

STDF Standard test data format

Test. Binary format for semiconductor test results and associated metadata.

STEP Standard for the exchange of product model data

PCB SI. ISO 10303 family used for exchanging product and mechanical geometry information.

STI Shallow trench isolation

Fabrication. Isolation structure whose geometry can also affect nearby device characteristics.

STIL Standard test interface language

Test. IEEE 1450 language for communicating digital test patterns and related test information.

STT-MRAM Spin-transfer torque MRAM

Architecture. MRAM switching magnetic states using spin-transfer torque.

STUMPS Self-testing using MISR and parallel shift-register sequence generator

Test. Logic BIST architecture combining parallel scan paths, pattern generation, and response compaction.

SUT System under test

Verification. Complete system being tested, including relevant hardware and software.

SV SystemVerilog

Languages. Hardware design and verification language standardized as IEEE 1800.

SVA SystemVerilog assertions

Verification. SystemVerilog constructs for specifying temporal and immediate properties.

SVD Singular value decomposition

AI/ML. Matrix factorization used in approximation, numerical analysis, and model reduction.

SVF Serial vector format

Test. Text format describing serial test operations, commonly for JTAG.

SVM Support vector machine

AI/ML. Learning model based on margin optimization and optionally kernel representations.

SVRF Standard verification rule format

Physical. Rule-deck language used by Siemens Calibre.

SVT Standard threshold voltage

Power. Intermediate threshold-voltage device or cell option; naming is foundry-specific.

SystemC SystemC

Languages. C++ class-library-based system modeling language; a name, not an acronym expansion.

SystemC AMS SystemC analog and mixed-signal extensions

Languages. Extensions for analog, mixed-signal, and heterogeneous system modeling.

SystemRDL System register description language

Languages. Language for describing registers and generating consistent implementation and documentation views.

T**Ta** Ambient temperature

Power. Temperature of the surrounding environment used in thermal conditions.

TAM Test access mechanism

Test. Infrastructure transporting test data and control to embedded cores or instruments.

TAP Test access port

Test. Standard test interface and controller associated with IEEE 1149.1.

TAT Turnaround time

Core. Elapsed time to complete a tool run, design iteration, or engineering process.

TB Testbench

Verification. Verification environment that stimulates a design and checks its responses.

TC Temperature coefficient

Analog RF. Rate of parameter change with temperature under a stated normalization.

TC Temperature cycling

Reliability. Reliability testing by repeated temperature changes.

TC Test coverage

Test. Test effectiveness metric whose treatment of untestable faults must be specified.

TCAD Technology computer-aided design

Devices. Simulation of semiconductor processes and device physics.

TCAM Ternary content-addressable memory

Architecture. CAM supporting zero, one, and don't-care match states.

TCK Test clock

Test. Clock signal for a JTAG test access port.

Tcl Tool command language

Languages. Scripting language widely used for EDA configuration, queries, constraints, and automation.

TCT Temperature cycling test

Reliability. Expanded abbreviation for temperature-cycle reliability testing.

Tddb Time-dependent dielectric breakdown

Reliability. Dielectric failure developing under sustained electrical stress.

TDF Transition delay fault

Test. Fault model representing excessively slow rising or falling signal transitions.

TDI Test data in

Test. Serial data input of a JTAG test access port.

TDO Test data out

Test. Serial data output of a JTAG test access port.

TDP Thermal design power

Power. Power level used for thermal design under a defined vendor or system convention.

TDR Test data register

Test. Data register used in a test-access or embedded-instrument network.

TDR Time-domain reflectometry

PCB SI. Measurement of impedance changes from reflected time-domain signals; distinct from test data register.

TDt Time-domain transmission

PCB SI. Measurement of a transmitted time-domain response through an interconnect.

TE Transverse electric

PCB SI. Mode with no electric-field component along the propagation direction.

TEE Trusted execution environment

Reliability. Isolated execution environment protecting selected code and data.

TEM Transmission electron microscopy

Fabrication. Imaging of electron transmission through thin specimens.

TEM Transverse electromagnetic

PCB SI. Propagation mode with electric and magnetic fields transverse to propagation; distinct from microscopy.

TF Transfer function

Analog RF. Relationship between an input perturbation and an output response.

TFET Tunnel field-effect transistor

Devices. Transistor using gate-controlled tunneling for carrier injection.

TGP Total graphics power

Power. Graphics-system power-budget terminology relevant to accelerator package and board design.

TGV Through-glass via

Packaging. Conductive connection passing through a glass substrate.

T/H Track and hold

Analog RF. Circuit that tracks an input before holding a sampled value.

THB Temperature humidity bias

Reliability. Reliability test applying temperature, humidity, and electrical bias.

THD Total harmonic distortion

Analog RF. Combined harmonic content relative to the fundamental signal.

THD+N Total harmonic distortion plus noise

Analog RF. Combined distortion and noise relative to a specified signal level.

THS Total hold slack

Timing. Aggregate hold slack metric, commonly summing violations; check report conventions.

THT Through-hole technology

PCB SI. Assembly method inserting component leads through board holes.

TIA Transimpedance amplifier

Analog RF. Amplifier converting input current to output voltage.

TID Total ionizing dose

Reliability. Cumulative ionizing-radiation exposure and associated device effects.

TIE Time interval error

PCB SI. Deviation of an edge time from a defined ideal or recovered timing reference.

TIM Thermal interface material

Packaging. Material reducing thermal resistance between contacting surfaces.

TIVA Thermally induced voltage alteration

Test. Failure-localization technique observing voltage changes caused by localized heating.

TJ Total jitter

PCB SI. Combined timing uncertainty evaluated at a stated error probability or measurement convention.

Tj Junction temperature

Power. Temperature of the semiconductor junction region; symbol rather than acronym.

TL Transfer learning

AI/ML. Reuse of learned representations or policies for another design task, circuit, or technology setting.

TLB Translation lookaside buffer

Architecture. Cache of address translations and associated permissions.

TLM Transaction-level modeling

Core. Modeling communication as transactions rather than every pin transition or clock cycle.

TLM-1 Transaction-level modeling version 1

Verification. SystemC transaction interface family also influential in UVM communication interfaces.

TLM-2.0 Transaction-level modeling version 2.0

Verification. SystemC transaction interfaces supporting generic payloads and standardized transport methods.

TLP Transaction layer packet

Interfaces. Packet exchanged by the PCIe transaction layer; distinct from transmission line pulse.

TLP Transmission line pulse

Reliability. Pulsed characterization method used for ESD protection and device behavior.

TM Transverse magnetic

PCB SI. Mode with no magnetic-field component along the propagation direction.

TMR Triple modular redundancy

Reliability. Three replicated computations with voting to tolerate specified faults.

TMS Test mode select

Test. JTAG signal controlling test-access-port state transitions.

TMV Through-mold via

Packaging. Conductive connection through package molding material.

TNS Total negative slack

Timing. Aggregate negative slack over reported endpoints or paths; aggregation rules are tool-dependent.

TPE Tree-structured Parzen estimator

Optimization. Density-model search method used for parameter tuning, including OpenROAD flow autotuning.

TPR True positive rate

AI/ML. Fraction of actual positives detected by a classifier; also called recall or sensitivity.

TPU Tensor processing unit

Architecture. Google accelerator-family name; also used loosely for tensor-oriented accelerators.

TQFP Thin quad flat package

Packaging. Thin-profile QFP package.

TR Track

Physical. Library or routing shorthand for track-based cell height or routing allocation; verify the stated convention.

TRAN Transient analysis

Analog RF. Time-domain circuit simulation; common command or analysis-name abbreviation.

TRNG True random number generator

Reliability. Generator deriving randomness from a physical entropy source.

TRST Test reset

Test. Optional JTAG controller reset signal; active-low notation commonly includes n or a bar.

TSO.ai Test space optimization AI

AI/ML. Synopsys AI application for semiconductor test optimization.

TSSOP Thin shrink small-outline package

Packaging. Fine-pitch thin-profile package family.

TSV Through-silicon via

Packaging. Conductive connection passing through a silicon substrate.

TT Typical-typical process corner

Timing. Nominal transistor-model corner; nominal does not imply every statistical average.

TTL Transistor-transistor logic

Interfaces. Bipolar logic family; also used to describe compatible I/O levels.

TTM Time to market

Core. Time required to move a product from development to commercial availability.

TTSC Test Technology Standards Committee

Ecosystem. IEEE committee overseeing test-related standards projects.

TVF Tcl verification format

Physical. Tcl-based rule-deck generation and extension mechanism used with Calibre.

U

uArch Microarchitecture

Architecture. Implementation organization realizing an instruction set or processing architecture.

UART Universal asynchronous receiver-transmitter

Interfaces. Hardware for asynchronous serial data transmission and reception.

UBM Under-bump metallization

Packaging. Metal stack providing interfaces between a die pad and bump connection.

uBump Microbump

Packaging. Fine-pitch bump connection for die stacking or high-density packaging.

UCDB Unified coverage database

Verification. Vendor database for storing and merging verification coverage results.

UCF User constraints file

Languages. Legacy Xilinx FPGA constraint format used by older implementation flows.

UCIe Universal chiplet interconnect express

Packaging. Standardized die-to-die interconnect architecture for chiplet integration.

UCIS Unified coverage interoperability standard

Verification. Standard interface and data model for exchanging verification coverage information.

UD Undetected fault

Test. ATPG classification for a fault not detected; exact categories are tool-specific.

UDIMM Unbuffered dual in-line memory module

Architecture. DIMM without the command/address register of an RDIMM.

UDN User-defined nettype

Verification. SystemVerilog nettype with user-defined data and optional resolution behavior, useful for real-number modeling.

UDP User-defined primitive

Verification. Verilog truth-table-defined logic or sequential primitive.

UDR User-defined resolution

Verification. User-specified resolution of multiple drivers on a SystemVerilog nettype; terminology is methodology-dependent.

UFS Universal flash storage

Interfaces. JEDEC storage-interface standard using a serial architecture.

UGB Unity-gain bandwidth

Analog RF. Frequency at which open-loop gain magnitude reaches unity.

UGF Unity-gain frequency

Analog RF. Alternative name for the unity-gain crossing frequency.

UI Unit interval

PCB SI. Duration of one symbol or bit interval as defined by the signaling convention.

UL Unsupervised learning

AI/ML. Learning structure without supplied target labels, for example grouping similar design runs or anomalies.

ULP Ultra-low power

Power. Context-dependent designation for very low power operation.

ULSI Ultra-large-scale integration

Core. Historical integration-scale term beyond VLSI; numerical thresholds are not universal.

ULVT Ultra-low threshold voltage

Power. Very low threshold-voltage option for performance-sensitive paths.

UMC Unbounded model checking

Formal. Property checking without limiting the proof to a fixed execution depth.

UNSAT Unsatisfiable

Formal. Result indicating that no assignment satisfies the given formula.

UPF Unified power format

Languages. Power-intent specification standardized by IEEE 1801.

UQ Uncertainty quantification

AI/ML. Quantification of prediction or model uncertainty, useful for deciding which circuit evaluations require further simulation.

URAM UltraRAM

FPGA. Large embedded memory resource in selected AMD FPGA families; a product-specific name.

USART Universal synchronous

asynchronous receiver-transmitter

Interfaces. Serial hardware supporting synchronous and asynchronous modes.

USB Universal serial bus

Interfaces. Host-controlled serial interconnect family for peripherals and devices.

USB-IF USB Implementers Forum

Interfaces. Organization supporting USB specifications and compliance programs.

UTBB Ultra-thin body and buried oxide

Devices. SOI structure with a thin semiconductor body and thin buried oxide.

UUT Unit under test

Verification. Hardware or subsystem being tested, particularly in production or laboratory contexts.

UVC UVM verification component

Verification. Reusable verification component constructed using UVM conventions.

UVM Universal verification methodology

Verification. Standardized SystemVerilog methodology and class library for reusable verification environments.

UVM-MS Universal verification

methodology for mixed-signal

Verification. Accellera methodology extending UVM concepts to mixed-signal verification.

UVVM Universal VHDL verification methodology

Verification. VHDL methodology and libraries for structured, reusable verification.

V

VAE Variational autoencoder

AI/ML. Generative model learning a probabilistic latent representation.

VBIC Vertical bipolar inter-company

Devices. Compact bipolar transistor model extending conventional Gummel-Poon modeling.

VBS Body-to-source voltage

Devices. Voltage difference between a MOS body and source.

VC Virtual channel

Interfaces. Logical channel sharing physical network links while maintaining separate flow-control state.

VCC Collector supply rail designation

Power. Conventional positive supply label originating in bipolar circuitry.

VCD Value change dump

Languages. Text format recording simulation value transitions over time.

VCO Voltage-controlled oscillator

Analog RF. Oscillator whose frequency is controlled by a voltage.

VCS VCS simulator

Ecosystem. Synopsys simulation product name; historical expansion is Verilog Compiled Simulator.

VCS Version control system

Ecosystem. System tracking revisions and collaboration; also a Synopsys simulator product name.

VCSEL Vertical-cavity surface-emitting laser

Photonics. Semiconductor laser emitting normal to the wafer surface.

VD Voltage domain

Power. Design region associated with a particular operating voltage.

VDD Positive supply rail designation

Power. Conventional MOS supply label, historically associated with drains; not necessarily the only positive rail.

VDMOS Vertical double-diffused MOS

Devices. Power MOS structure with a predominantly vertical current path.

VDS Drain-to-source voltage

Devices. Voltage difference between a transistor's drain and source terminals.

VEE Emitter supply rail designation

Power. Conventional supply label originating in bipolar circuitry, often a negative rail.

Verilog-A Verilog analog

Languages. Analog behavioral modeling subset used for circuit and device models.

Verilog-AMS Verilog analog and mixed-signal

Languages. Language combining analog modeling with event-driven digital descriptions.

VF Virtual function

Interfaces. Lightweight PCIe function exposed for I/O virtualization.

VF-TLP Very-fast transmission line pulse

Reliability. TLP method using very fast pulses for short-timescale ESD characterization.

VGA Variable-gain amplifier

Analog RF. Amplifier with controllable gain.

VGS Gate-to-source voltage

Devices. Voltage difference between a transistor's gate and source terminals.

VHDL VHSIC hardware description language

Languages. Hardware description language standardized as IEEE 1076; VHSIC expands separately.

VHDL-AMS VHDL analog and mixed-signal extensions

Languages. IEEE 1076.1 extensions for analog and mixed-signal modeling.

VHPI VHDL procedural interface

Languages. Standard procedural access to VHDL simulation objects and operations.

VHSIC Very high speed integrated circuit

Languages. Historical program name embedded in the expansion of VHDL.

VIO Virtual input and output

FPGA. FPGA debug IP for observing and controlling internal signals.

VIP Verification intellectual property

Verification. Reusable verification components for interfaces, protocols, or functional blocks.

VIPPO Via in pad plated over

PCB SI. PCB construction with a via in a component pad and a plated-over surface.

VLIW Very long instruction word

Architecture. Architecture encoding multiple operations for parallel issue in one instruction word.

VLM Vision-language model

AI/ML. Model processing both visual and textual inputs, potentially including layouts and schematics.

VLSI Very-large-scale integration

Core. Integration of large numbers of devices into a single integrated circuit.

VMM Verification methodology manual

Verification. Historical verification methodology and library associated with Synopsys.

VNA Vector network analyzer

PCB SI. Instrument measuring complex network responses, typically scattering parameters.

VP Virtual platform

Verification. Integrated executable hardware-model environment for software development and system validation.

VP Virtual prototype

Verification. Executable system model used before physical hardware is available.

VPD VCD plus

Languages. Proprietary simulation waveform database format associated with Synopsys VCS.

VPI Verilog procedural interface

Languages. Object-oriented procedural access interface to Verilog and SystemVerilog simulation data.

VS Variable shaped beam

Fabrication. Electron-beam writing approach using controllable shaped shots.

VSO.ai Verification space optimization AI

AI/ML. Synopsys AI application for verification optimization and coverage efficiency.

VSS Reference supply rail designation

Power. Conventional MOS return-rail label, historically associated with sources; often ground.

VSWR Voltage standing-wave ratio

PCB SI. Standing-wave amplitude ratio associated with transmission-line mismatch.

VT Threshold voltage

Devices. Gate-voltage parameter associated with channel turn-on under a specified extraction convention.

Vth Threshold voltage

Devices. Alternative notation for VT.

VTS VLSI Test Symposium

Ecosystem. Conference on integrated-circuit and system test research.

VUnit VUnit

Verification. Open-source HDL unit-test framework; a project name.

W**W2W** Wafer to wafer

Packaging. Bonding or integration of complete wafers.

WA Weighted average

Optimization. Smooth wirelength model used by analytical placers; here a model-specific abbreviation rather than any weighted mean.

WAT Wafer acceptance test

Fabrication. Electrical process-monitoring tests used to assess wafer fabrication quality.

WBR Wrapper boundary register

Test. Test wrapper register providing boundary control and observation.

WBY Wrapper bypass register

Test. Register providing a short serial path when a wrapper is bypassed.

WC Worst case

Timing. Pessimistic analysis condition; setup, hold, leakage, and power can have different worst cases.

WDM Wavelength-division multiplexing

Photonics. Transmission of multiple channels using different optical wavelengths.

WGL Waveform generation language

Test. Test-pattern representation used in semiconductor test flows.

WHS Worst hold slack

Timing. Worst slack among the hold checks included in a report.

WIR Wrapper instruction register

Test. Instruction register controlling a test wrapper, such as an IEEE 1500 wrapper.

WLCSP Wafer-level chip-scale package

Packaging. Wafer-level package with dimensions close to those of the die.

WLF Wave log format

Languages. Waveform database format associated with ModelSim and Questa simulation.

WLM Wire-load model

Timing. Statistical wire-parasitic estimate used when placement or routing information is unavailable.

WLP Wafer-level packaging

Packaging. Packaging processes performed substantially at wafer level.

WNS Worst negative slack

Timing. Worst failing timing slack; report conventions for passing designs vary.

WPE Well proximity effect

Physical. Device-parameter change associated with proximity to well boundaries.

WPS Worst pulse-width slack

Timing. Worst margin against a minimum pulse-width requirement.

WS Wafer sort

Test. Wafer-level electrical test used to classify dies.

X**XAG** XOR-and graph

Formal. Logic graph using XOR and AND nodes, typically with complemented edges.

XAI Explainable artificial intelligence

AI/ML. Methods for inspecting model behavior and feature influence, supporting interpretation of EDA predictions and decisions.

XDC Xilinx design constraints

Languages. AMD FPGA constraint format based on Tcl, including timing and physical constraints.

X-fill Unknown-bit filling

Test. Assignment of unspecified test-cube bits for compression, power, or coverage objectives.

XGBoost Extreme gradient boosting

AI/ML. Machine-learning library and boosting implementation; a project name.

XGMII 10-gigabit media-independent interface

Interfaces. Interface between 10-gigabit Ethernet MAC and PHY functions.

XMG XOR-majority graph

Formal. Logic graph using XOR and majority operators.

XML Extensible markup language

Languages. Structured text representation used by IP metadata and many tool interchange files.

XMR Cross-module reference

Verification. Hierarchical reference to an object outside the current HDL module or scope.

XPM Xilinx parameterized macros

Verification. Reusable parameterized macros for memory, clock-domain crossing, and related FPGA functions.

X-prop Unknown-value propagation
Verification. Simulation treatment of unknown logic values; semantics depend on language and tool options.

XPS X-ray photoelectron spectroscopy
Fabrication. Surface-composition and chemical-state analysis using emitted photoelectrons.

XSVF Xilinx serial vector format
Test. Compact binary derivative of SVF associated with device programming flows.

Y

YAML YAML Ain't Markup Language
Languages. Configuration serialization language used in some EDA flows and infrastructure.

Z

ZCS Zero-current switching
Analog RF. Switching arranged near zero device current to reduce switching loss.

ZDD Zero-suppressed decision diagram
Formal. Decision diagram representation useful for sparse set families.

ZeBu Zero bugs
Ecosystem. Historical expansion of the EVE hardware-emulation product name, now a Synopsys product family; a brand origin, not a claim of defect-free designs.

Zth Thermal impedance
Power. Time- or frequency-dependent thermal response relating power and temperature rise.

ZVS Zero-voltage switching
Analog RF. Switching arranged near zero device voltage to reduce switching loss.

Ambiguity guide

These headwords have multiple meanings in this dictionary. Use the domain and surrounding nouns to resolve the intended sense.

ABIST

Analog built-in self-test (Test); Array built-in self-test (Test).

AXI

Advanced extensible interface (Interfaces); Automated X-ray inspection (PCB SI).

CAM

Computer-aided manufacturing (Core); Content-addressable memory (Architecture).

CCI

Camera control interface (Interfaces); Configuration control and inspection (Languages).

CCS

Camera command set (Interfaces); Composite current source (Timing).

CD

Continuous delivery (Ecosystem); Critical dimension (Fabrication).

CG

Clock gating (Power); Conjugate gradient (Optimization).

CML

Compact model library (Photonics); Current-mode logic (Interfaces).

CP

Charge pump (Analog RF); Chip probing (Test); Clock pin (Timing).

CTL

Computation tree logic (Formal); Core test language (Test).

DAC

Design Automation Conference (Ecosystem); Digital-to-analog converter (Analog RF).

DBI

Data bus inversion (Architecture); Direct bond interconnect (Packaging).

DC

Design Compiler (Ecosystem); Diagnostic coverage (Reliability); Direct current (Analog RF); Don't care (Formal).

DCM

Digital clock manager (FPGA); Discontinuous conduction mode (Analog RF).

DCP

Design checkpoint (FPGA); Disciplined convex programming (Optimization).

DFA

Dependent failure analysis (Reliability); Design for assembly (PCB SI); Differential fault analysis (Reliability).

DFD

Design for debug (Physical); Design for diagnosis (Test).

DFT

Density functional theory (Devices); Design for testability (Test); Discrete Fourier transform (AI/ML).

DFX

Design for X (Physical); Dynamic function exchange (FPGA).

DL

Deep learning (AI/ML); Defect level (Test).

DP

DisplayPort (Interfaces); Double patterning (Fabrication); Dynamic programming (Optimization).

DR

Data register (Test); Detailed routing (Physical).

DSP

Digital signal processing (Architecture); Digital signal processor (Architecture).

DUV

Deep ultraviolet (Fabrication); Design under verification (Verification).

EM

Electromagnetic (PCB SI); Electromigration (Reliability).

EOT

End of test (Test); Equivalent oxide thickness (Devices).

ESL

Electronic system level (Core); Equivalent series inductance (Analog RF).

FC

Fault coverage (Test); Functional coverage (Verification); Fusion Compiler (Ecosystem).

FF

Fast-fast process corner (Timing); Flip-flop (FPGA).

FM

Fiduccia-Mattheyses (Optimization); Formality (Ecosystem).

FP

False path (Timing); Floorplanning (Physical).

FSR

Free spectral range (Photonics); Full-scale range (Analog RF).

FV

Formal verification (Formal); Functional verification (Verification).

GP

Gaussian process (AI/ML); Geometric programming (Optimization).

HB

Harmonic balance (Analog RF); Hybrid bonding (Packaging).

HBM

High-bandwidth memory (Architecture); Human body model (Reliability).

ICL

In-context learning (AI/ML); Instrument connectivity language (Test).

IDE

Integrated development environment (Ecosystem); Integrity and data encryption (Interfaces).

IOB

Input-output block (FPGA); Input-output buffer (FPGA).

IP

Integer programming (Optimization); Intellectual property (Core).

IPC

Instructions per cycle (Architecture); Interprocess communication (Ecosystem); IPC standards designation (Ecosystem).

IR

Instruction register (Test); Intermediate representation (Languages).

ISO

International Organization for Standardization (Ecosystem); Isolation (Power).

LP

Linear programming (Optimization); Low power (Power).

MAC

Media access control (Interfaces); Multiply accumulate (Architecture).

MCP

Model context protocol (AI/ML); Multi-chip package (Packaging); Multicycle path (Timing).

MCU

Microcontroller unit (Architecture);
Multiple-cell upset (Reliability).

MDP

Markov decision process (AI/ML); Mask
data preparation (Fabrication).

MPU

Memory protection unit (Architecture);
Microprocessor unit (Architecture).

MPW

Minimum pulse width (Timing); Multi-
project wafer (Core).

MSI

Medium-scale integration (Core); Message-
signaled interrupt (Interfaces).

NCO

Neural combinatorial optimization (AI/ML);
Numerically controlled oscillator (Analog
RF).

NLP

Natural language processing (AI/ML);
Nonlinear programming (Optimization).

OCP

Open Compute Project (Ecosystem); Open
core protocol (Ecosystem).

PCA

Principal component analysis (AI/ML);
Printed circuit assembly (PCB SI).

PCM

Phase-change memory (Architecture);
Process control monitor (Fabrication).

PD

Photodetector (Photonics); Physical design
(Physical); Power delivery (Interfaces);
Power domain (Power).

PG

Power and ground (Physical); Power gating
(Power).

PGA

Pin grid array (Packaging); Programmable-
gain amplifier (Analog RF).

PR

Partial reconfiguration (FPGA); Precision-
recall (AI/ML).

PSM

Phase-shift mask (Fabrication); Pulse-
skipping mode (Analog RF).

PSS

Periodic steady state (Analog RF); Portable
test and stimulus standard (Verification).

RET

Resolution enhancement technology
(Fabrication); Retention (Power).

RF

Radio frequency (Analog RF); Random
forest (AI/ML); Register file (Architecture).

RL

Reinforcement learning (AI/ML); Return
loss (PCB SI).

ROM

Read-only memory (Architecture);
Reduced-order model (AI/ML).

SAC

Self-aligned contact (Fabrication); Soft
actor-critic (AI/ML).

SDC

Satisfiability don't care (Formal); Synopsys
design constraints (Languages).

SDF

Standard delay format (Languages);
Synchronous dataflow (Verification).

SI

International System of Units (Ecosystem);
Signal integrity (PCB SI).

SLM

Silicon lifecycle management (Test); Small
language model (AI/ML).

SMT

Satisfiability modulo theories (Formal);
Surface-mount technology (PCB SI).

SOA

Safe operating area (Reliability);
Semiconductor optical amplifier
(Photonics).

SS

Slow-slow process corner (Timing);
Subthreshold swing (Devices).

SSL

Self-supervised learning (AI/ML); Semi-
supervised learning (AI/ML).

SSN

Simultaneous switching noise (PCB SI);
Streaming scan network (Test).

TC

Temperature coefficient (Analog RF);
Temperature cycling (Reliability); Test
coverage (Test).

TDR

Test data register (Test); Time-domain
reflectometry (PCB SI).

TEM

Transmission electron microscopy
(Fabrication); Transverse electromagnetic
(PCB SI).

TLP

Transaction layer packet (Interfaces);
Transmission line pulse (Reliability).

VCS

VCS simulator (Ecosystem); Version control
system (Ecosystem).

VP

Virtual platform (Verification); Virtual
prototype (Verification).

Case and naming distinctions

DK and Dk

DK means design kit. Dk denotes dielectric
constant in PCB usage.

EDP and eDP

EDP is energy-delay product. eDP means
Embedded DisplayPort.

GAN and GaN

GAN is a generative adversarial network.
GaN denotes gallium nitride.

GM and Gm

GM is gain margin. Gm denotes
transconductance.

TJ and Tj

TJ means total jitter. Tj denotes junction
temperature.

S/D and SD

S/D denotes source and drain. SD identifies
Secure Digital memory-card standards;
punctuation matters.

SIP and SiP

SIP commonly means semiconductor
intellectual property. SiP means system in
package. Case is useful, but source
documents may not preserve it.

SOIC and SolC

SOIC identifies a small-outline package.
TSMC SolC names a three-dimensional
integration technology.

SPF and SPEF

SPEF is Standard Parasitic Exchange Format.
SPF is a different parasitic-format family,
including DSPF and RSPF.

LEF and DEF

LEF mainly supplies technology and library
abstractions. DEF supplies design-instance
physical information.

SDC and SDF

SDC states design constraints. SDF
communicates delays and timing checks for
uses such as simulation back-annotation.

PSS and UPF

PSS can mean portable test and stimulus or
periodic steady state. UPF describes power
intent; it is neither of those PSS concepts.

MCMM and MMMC

These are alternative word orders for multi-corner multi-mode analysis rather than different analysis classes.

CPPR and CRPR

Both concern timing pessimism associated with shared or reconvergent clock paths. Exact scope and naming vary between tools.

DFT and test coverage

Design for testability is distinct from Fourier transforms and density functional theory. Fault coverage and test coverage also require explicit denominator conventions.

IR and IR drop

IR can mean intermediate representation or instruction register. In IR drop, I and R are current and resistance symbols.

AI products and methods

DSO.ai, VSO.ai, TSO.ai, and ASO.ai are product names. RL, BO, and GNN name method families and do not imply a particular product implementation.

Domain index

Find neighboring vocabulary by engineering activity. Each headword links to its first entry in this domain. Reference codes lead to the primary-reference section.

Core

Foundations and design flow. 52 entries (52 headwords).

ADK, ASIC, ASIP, ASSP, BE, BEOL, BoM, CAD, CAE, CAM, DK, DTCO, ECAD, ECO, EDA, ESL, FCO, FE, FEOL, GDS-to-silicon, HDL, HLD, HLS, HVL, IC, IDM, IP, KPI, LSI, MOL, MPW, MSI, NRE, ODM, OEM, OSAT, PDK, PPA, PPAC, QoR, RTL, RT-level, RTL-to-GDSII, SIP, SoC, SSI, STCO, TAT, TLM, TTM, ULSI, VLSI.

Primary reading: R05, R07, R08, R18, R19

Languages

Languages formats and design databases. 72 entries (72 headwords).

ALF, API, AST, BENCH, BLIF, BNF, CCI, CDL, CIF, CIRCT, CPF, CSV, DB, DEF, DPI, DPI-C, DSPF, EBLIF, EBNF, EDIF, EVCD, FIRRTL, FLI, FSDB, FSL, FST, GDSII, IPSA, IP-XACT, IR, JSON, LEF, LIB, LRM, MLIR, NDM, OA, OASIS, OASIS.MASK, OpenDB, PLI, QPF, QSF, RSPF, RTLIL, SA-EDI, SAIF, SDC, SDF, SKILL, SPEF, SPF, SV, SystemC, SystemC AMS, SystemRDL, Tcl, UCF, UPF, VCD, Verilog-A, Verilog-AMS, VHDL, VHDL-AMS, VHPI, VHSIC, VPD, VPI, WLF, XDC, XML, YAML.

Primary reading: R01, R02, R13, R14, R16, R39, R87

Verification

Functional verification and simulation. 59 entries (58 headwords).

ABV, AT, BA, BFM, CC, CDC, CDV, cocotb, CRTP, CRV, DES, DMI, DUT, DUV, DV, eRM, FC, FSM, FV, GLS, ICE, ISS, LT, MC/DC, MDV, NBA, OOP, OSVVM, OVL, OVM, PSL, PSS, RAL,

RDC, SCE-MI, SDF, SUT, SVA, TB, TLM-1, TLM-2.0, UCDB, UCIS, UDN, UDP, UDR, UUT, UVC, UVM, UVM-MS, UVVM, VIP, VMM, VP, VUnit, XMR, XPM, X-prop.

Primary reading: R01, R02, R03, R04, R25

Formal

Formal methods and logic synthesis. 48 entries (48 headwords).

ABC, AG, AIG, ALAP, ASAP, BDD, BMC, CDFG, CEC, CEGAR, CEX, CFG, CNF, COI, CTL, CTL*, DAG, DC, DFG, DNF, EXDC, FEV, FPV, FV, IC3, II, L2S, LEC, LTL, LUT, MIG, ODC, PDR, POS, QBF, ROBDD, SAT, SCC, SDC, SEC, SIS, SMT, SOP, UMC, UNSAT, XAG, XMG, ZDD.

Primary reading: R14, R15, R02, R88

Timing

Timing and library characterization. 61 entries (61 headwords).

AOCV, BC, CCB, CCS, CK, CKQ, CLK, Cmax, Cmin, CP, CPPR, CQ, CRPR, DMSA, DTA, ECSM, ETM, FF, Fmax, Fmin, FO, FO4, FP, FS, GBA, ILM, I/O, LVF, MCMM, MCP, MMMC, MPW, NLDM, NLM, NLPM, NVP, OC, OCV, PBA, POCV, PVT, PVTA, QTM, RC, RCmax, RCmin, RLC, SF, Slew, SOCV, SS, SSTA, STA, THS, TNS, TT, WC, WHS, WLM, WNS, WPS.

Primary reading: R06, R09, R05

For synchronizer reliability, see MTBF in Reliability.

Physical

Physical implementation and signoff. 57 entries (57 headwords).

APR, BPR, BSPDN, CCOpt, CTO, CTS, DBU, DFD, DFM, DFR, DFV, DFX, DFY, DIR, DR, DRC, DRD, DRM, DRV, EMIR, ERC, FLUTE, FP, GCell, GR, HPWL, H-tree, IR-drop, LDE, LI, LOD, LPE, LRC, LVS, M1, MMP, MSCTS, MST, NDR, PD, PDN, PERC, PEX, PG, PGN, PnR, P&R, RCX, RMST, RSMT, RUDY, RVE, SIR, SVRF, TR, TVF, WPE.

Primary reading: R08, R10, R11, R12, R18

Power

Power intent and power management. 47 entries (47 headwords).

ABB, AO, AON, AVFS, AVS, CG, DFS, DVFS, DVS, ED2P, EDP, FBB, HVT, ICG, ISO, LP, LS, LVT, MSV, MTCMOS, MV, PD, PDP, PG, PMIC, PMU, PST, RBB, RET, RFF, Rth, RVT, SLVT, SRPG, SVT, Ta, TDP, TGP, Tj, ULP, ULVT, VCC, VD, VDD, VEE, VSS, Zth.

Primary reading: R02, R05, R07

Analog RF

Analog mixed signal and RF. 112 entries (112 headwords).

AC, ACLR, ACPR, ADC, ADPLL, AGC, AMS, BB, BGR, BPF, BSF, BW, CCM, CDR, CMFB, CMRR, CP, CTAT, DAC, DC, DCM, DCO, DLL, DMS, DNL, DSM, EEnet, ENOB, ESL, ESR, EVM, FastSPICE, FLL, FSR, GBW, GM, Gm-C, HB, HPF, IF, IIP3, IMD, INL, IP3, IP3, I/Q, LDO, LNA, LO, LPF, LSB, MC, MMIC, MS, MSB, NCO, NF, OIP3, OP, OPA, OSR, OTA, P1dB, PA, PAC, PAE, PFD, PFM, PGA, PLL, PM, PNoise, PSM, PSRR, PSS, PSTB, PTAT, PWM, PXF, PZ, Q, QPNOISE, QPSS, RF, RFIC, RNM, SAR, SC, SDM, SFDR, S/H, SHA, SINAD, SMPS, SNDR, SNR, SPICE, SR, STB, TC, TF, T/H, THD, THD+N, TIA, TRAN, UGB, UGF, VCO, VGA, ZCS, ZVS.

Primary reading: R20, R21, R23, R24, R25, R87

Devices

Semiconductor devices and compact models. 73 entries (73 headwords).

BCD, BiCMOS, BJT, BOX, BSIM, BSIM-CMG, BSIM-IMG, BSIM-SOI, BTBT, CET, CFET, CGP, CLM, CMOS, CPP, DD, DFT, DIBL, DMOS, EKV, EOT, FD-SOI, FeFET, FET, FinFET, GAA, GaAs, GaN, Gds, GIDL, Gm, HBT, HD, HEMT, HICUM, HiSIM, HKMG, Ids, IGBT, IGFET, JFET, LDMOS, MOS, MOSFET, NCFET, NEGF, NMOS, NPN, NSFET, NWFET, PD-SOI, pHEMT, PMOS, PNP,

PSP, RTN, RTS, SCE, SiC, SiGe, SOI, SRH, SS, TCAD, TFET, UTBB, VBIC, VBS, VDMOS, VDS, VGS, VT, Vth.

Primary reading: R18, R21, R22, R17

Fabrication

Fabrication lithography and metrology. 71 entries (71 headwords).

AFM, ALD, ALE, APC, CD, CD-SEM, CDU, CMP, CVD, DOE, DOF, DP, DPT, DRIE, DSA, DUV, EBL, EDS, EDX, EPE, EUV, FDC, FIB, High-NA, ICP, ILT, LDD, LELE, LELELE, LER, LOCOS, LPCVD, LWR, MBE, MDP, MEB, MEEF, MOCVD, MPC, MRC, NA, NILS, OCD, OPC, PCM, PECVD, PSM, PVB, PVD, PW, R2R, RET, RIE, RMG, RTA, RTP, SAB, SAC, SADP, SAQP, S/D, SEM, SIMS, SMO, SPC, SRAF, STI, TEM, VSB, WAT, XPS.

Primary reading: R17, R26, R27

Test

Design for test and silicon debug. 92 entries (91 headwords).

ABIST, ATDF, ATE, ATPG, AU, BILBO, BIRA, BISR, BIST, BSDI, BSR, CP, CTL, DFD, DFT, DL, DPMO, DPPM, DR, DT, EBAC, EBIC, EDT, EFA, EMMI, EOT, FA, FC, FT, ICL, IDDQ, IDDT, IJTAG, IR, IST, JTAG, KGD, LBIST, LFSR, LIVA, LOC, LOS, LSSD, LVP, MBIST, MISR, N-detect, OBIRCH, OCC, OCI, OPCI, PBIST, PDF, PDL, PFA, POST, PRPG, SA0, SA1, SAF, SCOAP, SDD, SIB, SISR, SLM, SLT, SOT, SSN, STDF, STIL, STUMPS, SVF, TAM, TAP, TC, TCK, TDF, TDI, TDO, TDR, TIVA, TMS, TRST, UD, WBR, WBY, WGL, WIR, WS, X-fill, XSUF.

Primary reading: R28, R29, R30, R31, R32, R33, R34, R35

Reliability

Reliability safety and hardware security. 76 entries (75 headwords).

ASIL, BTI, CCF, CDM, CMF, CPA, CRC, DC, DDD, DFA, DICE, DMR, DPA, ECC, EDC, EM, EOS, ESD, FI, FIT, FMEA, FMEDA, FTA, FTTI, GLIFT,

HAST, HBM, HCD, HCI, HRoT, HSM, HT, HTGB, HTOL, HTRB, IFT, LET, LFM, MBU, MCU, MM, MTBF, MTTF, NBTI, PBTI, PMHF, PRNG, PUF, QM, RHBD, RHBP, RoT, SCA, SEB, SECDDED, SEE, SEFI, SEGR, SEL, SER, SET, SEU, SIL, SOA, SPFM, TC, TCT, TDDb, TEE, THB, TID, TLP, TMR, TRNG, VF-TLP.

Primary reading: R36, R37, R38, R28

Packaging

Packaging chiplets and heterogeneous integration. 61 entries (61 headwords).

2.5D, 3D-IC, 3DIC, AIB, AiP, B2B, BGA, BoW, C2C, C4, CoWoS, CSAM, CSP, CTE, CTI, Cu-Cu, D2D, D2W, DBI, DFN, DIP, EMIB, F2B, F2F, FBGA, FCBGA, FOPLP, Foveros, FOWLP, HB, HBI, HI, InFO, IPD, LGA, MCM, MCP, MSL, PGA, PiP, PoP, QFN, QFP, RDL, SAM, SiP, SOIC, SoIC, SoW, TGV, TIM, TMV, TQFP, TSSOP, TSV, UBM, uBump, UCle, W2W, WLCSP, WLP.

Primary reading: R41, R42, R43, R44, R45

PCB SI

PCB signal integrity and electromagnetic analysis. 85 entries (85 headwords).

AMI, AOI, AXI, BEM, BER, BERT, BUJ, COM, CPW, CTLE, DCD, DDJ, Df, DFA, DFE, DJ, Dk, EM, EMC, EMC/EMI, EMI, EMS, FDTD, FEC, FEM, FEXT, FFE, FIR, GCPW, HDI, IBIS, IBIS-AMI, IBIS-ISS, ICM, ICT, IDF, IDX, IIR, IL, IPC-2581, IPC-D-356, ISI, MCAD, MoM, NEXT, NPTH, NRZ, NRZI, ODB++, PAM, PAM4, PCA, PCB, PCBA, PEEC, PER, PI, PIH, PJ, PRBS, PTH, PWB, RJ, RL, RLGC, RMS, SI, SMD, SMT, S-parameter, SSN, SSO, STEP, TDR, TDT, TE, TEM, THT, TIE, TJ, TM, UI, VIPPO, VNA, VSWR.

Primary reading: R39, R40, R65

Interfaces

Interfaces protocols and on chip interconnect. 98 entries (98 headwords).

ACE, AHB, AMBA, APB, A-PHY, ASB, ATA, ATB, ATS, AXI, AXI4-Lite, AXI4-Stream, BAR, BDF, CAN, CAN FD, CCI, CCIX, CCS, CHI, CHI C2C,

CML, C-PHY, CSI, CXL, DLLP, DP, D-PHY, DSC, DSI, DTI, ECL, eDP, eMMC, FLIT, GMII, HDMI, HOL, HSTL, I2C, I2S, I3C, IDE, LIN, LTSSM, LVCMOS, LVDS, LVPECL, LVTTTL, MAC, MDC, MDIO, MIPI, M-PHY, MSI, MSI-X, NIU, NoC, NVMe, OSPI, PASID, PCI, PCIe, PCI-SIG, PCS, PD, PECL, PF, PHY, PIPE, PMA, PMD, PRI, QoS, QSPI, RFFE, RGMII, SAS, SATA, SCSI, SD, SDIO, SerDes, SGMII, SLIMbus, SPI, SR-IOV, SSTL, TLP, TTL, UART, UFS, USART, USB, USB-IF, VC, VF, XGMII.

Primary reading: R46, R47, R48, R49, R50, R51

Architecture

Processors architecture and memory. 98 entries (96 headwords).

AGU, AIMC, ALU, CA, CAM, CIM, CISC, CKE, CPI, CPU, CSR, DBI, DDR, DIMM, DMA, DPU, DQ, DQS, DRAM, DSP, EEPROM, eFuse, EPROM, FeRAM, FIFO, FMA, FPU, FRAM, GDDR, GPU, HBM, HMC, IMC, IOMMU, IPC, ISA, L1, L2, L3, LIFO, LLC, LPDDR, LRDIMM, LSQ, MAC, MCU, MESI, MIMD, MMIO, MMU, MOESI, MPU, MRAM, MSHR, MSR, NPU, NVM, NVRAM, ODT, OOO, OTP, PC, PCM, PCRAM, PIM, PROM, PTE, PTW, RAM, RAS, RCD, RDIMM, ReRAM, RF, RISC, RISC-V, RMW, ROB, ROM, RRAM, SDRAM, SIMD, SIMT, SMMU, SODIMM, SOT-MRAM, SP, SPD, SRAM, STT-MRAM, TCAM, TLB, TPU, uArch, UDIMM, VLIW.

Primary reading: R47, R52, R53

FPGA

FPGA and programmable logic. 47 entries (46 headwords).

ALM, BIT, BRAM, BUFG, BUFGCE, BUFR, CGRA, CLB, CPLD, DCM, DCP, DFF, DFX, eFPGA, FF, FPGA, GAL, GT, HPS, ICAP, ILA, IOB, IOE, IOLOGIC, JIC, JTAG-to-AXI, LAB, LC, LE, MLAB, MMCM, OOC, PAL, PCAP, PL, PLA, PLD, POF, PR, PS, RBF, RBT, SOF, SRL, URAM, VIO.

Primary reading: [R54](#), [R55](#), [R56](#), [R90](#)

Optimization

Optimization methods for EDA. 49 entries (49 headwords).

[ADMM](#), [B&B](#), [B&C](#), [BFGS](#), [BO](#), [CG](#), [CMA-ES](#), [DCP](#), [DE](#), [DFO](#), [DP](#), [DSE](#), [EA](#), [EHVI](#), [EI](#), [FM](#), [GA](#), [GD](#), [GP](#), [HPO](#), [HV](#), [ILP](#), [IP](#), [KKT](#), [KL](#), [L-BFGS](#), [L-BFGS-B](#), [LM](#), [LP](#), [LSE](#), [MILP](#), [MIP](#), [MIQP](#), [MOBO](#), [MOO](#), [NAG](#), [NCG](#), [NLP](#), [NSGA-II](#), [PSO](#), [QP](#), [SA](#), [SBO](#), [SDP](#), [SMBO](#), [SOCP](#), [SQP](#), [TPE](#), [WA](#).

Primary reading: [R66](#), [R67](#), [R68](#), [R69](#), [R70](#), [R71](#), [R72](#), [R73](#), [R74](#), [R75](#), [R76](#), [R77](#), [R85](#), [R86](#)

AI/ML

AI ML and supporting numerical methods for EDA. 103 entries (102 headwords).

[AD](#), [AE](#), [AI](#), [AL](#), [AMG](#), [ANN](#), [ASO.ai](#), [AUC](#), [AWE](#), [CNN](#), [CUDA](#), [DA](#), [DAE](#), [DAPT](#), [DCT](#), [DFT](#), [DL](#), [DNN](#), [DQN](#), [DRL](#), [DSO.ai](#), [FFT](#), [FMM](#), [FNR](#), [FPR](#), [GAN](#), [GAT](#), [GBDT](#), [GCN](#), [GEMM](#), [GenAI](#), [GIN](#), [GMRES](#), [GNN](#), [GP](#), [GPR](#), [GRU](#), [HGNN](#), [ICL](#), [IFFT](#), [LLM](#), [LLMOps](#), [LoRA](#), [LSTM](#), [LU](#), [MAE](#), [MAPE](#), [MCP](#), [MDP](#), [ML](#), [MLOps](#), [MLP](#), [MNA](#), [MOR](#), [MPNN](#), [MSE](#), [NAS](#), [NCO](#), [NLP](#), [NN](#), [NR](#), [ODE](#), [ONNX](#), [OOD](#), [PBT](#), [PCA](#), [PCG](#), [PDE](#), [PEFT](#), [POD](#), [POMDP](#), [PPO](#), [PR](#), [PRIMA](#), [RAG](#), [RF](#), [RL](#), [RLHF](#), [RMSE](#), [RNN](#), [ROC](#), [ROM](#), [SAC](#), [SFT](#), [SGD](#), [SL](#), [SLM](#), [SpMM](#), [SpMV](#), [SSL](#), [SVD](#), [SVM](#), [TL](#), [TPR](#), [TSO.ai](#), [UL](#), [UQ](#), [VAE](#), [VLM](#), [VSO.ai](#), [XAI](#), [XGBoost](#).

Primary reading: [R78](#), [R80](#), [R81](#), [R82](#), [R83](#), [R84](#), [R79](#), [R57](#), [R58](#), [R59](#), [R60](#), [R61](#)

Photonics

Photonics MEMS and multiphysics. 44 entries (44 headwords).

[APD](#), [AWG](#), [BAW](#), [BPM](#), [CFD](#), [CHT](#), [CML](#), [CPO](#), [CWDM](#), [DBR](#), [DFB](#), [DWDM](#), [EAM](#), [EC](#), [EIC](#), [EME](#), [EPIC](#), [ER](#), [FBAR](#), [FDE](#), [FEA](#), [FSI](#), [FSR](#), [GC](#), [MEMS](#), [MMI](#), [MOEMS](#), [MRR](#), [MZI](#), [MZM](#), [NEMS](#), [NPO](#), [OIO](#), [OSNR](#), [PD](#), [PIC](#), [PIN](#), [RCWA](#), [SAW](#), [SiPh](#), [SOA](#), [SPAD](#), [VCSEL](#), [WDM](#).

Primary reading: [R62](#), [R63](#), [R64](#), [R20](#)

Ecosystem

Tools infrastructure organizations and conferences. 69 entries (66 headwords).

[ADE](#), [ADS](#), [AMS Designer](#), [ASP-DAC](#), [AWR](#), [CD](#), [CI](#), [CLI](#), [CST](#), [DAC](#), [DASC](#), [DATE](#), [DC](#), [DRMAA](#), [DVCon](#), [EMX](#), [ESDA](#), [ESD Alliance](#), [ETS](#), [FC](#), [FM](#), [GSA](#), [GUI](#), [HAPS](#), [HFSS](#), [HPC](#), [HSPICE](#), [IaaS](#), [IaC](#), [ICC](#), [ICC2](#), [ICCAD](#), [ICV](#), [IDE](#), [IEC](#), [IEDM](#), [IEEE](#), [IPC](#), [IRDS](#), [ISO](#), [ISPD](#), [ISQED](#), [ISSCC](#), [ITC](#), [ITRS](#), [JEDEC](#), [LSF](#), [MPI](#), [OCP](#), [ODSA](#), [OpenMP](#), [OSFP](#), [PT](#), [PX](#), [Q3D](#), [QSFP](#), [REST](#), [RPC](#), [SaaS](#), [SEMI](#), [SI](#), [Si2](#), [TTSC](#), [VCS](#), [VTS](#), [ZeBu](#).

Primary reading: [R01](#), [R02](#), [R05](#), [R28](#), [R65](#), [R89](#), [R90](#), [R91](#), [R92](#), [R93](#), [R94](#)

Optimization and AI ML cross references

Optimization entries describe methods used in circuit sizing, partitioning, placement, implementation, and flow tuning. AI/ML entries cover EDA predictors, learned representations, search policies, and engineering assistance. Related objectives, metrics, and physical techniques retain their existing domain tags.

Objectives and closure: [PPA](#), [PPAC](#), [QoR](#), [WNS](#), [TNS](#), [EDP](#), [PDP](#), [HPWL](#).

Design and implementation: [DTCO](#), [STCO](#), [ECO](#), [CCOpt](#), [CTO](#), [CTS](#), [PnR](#).

Learning and optimization: [BO](#), [GP](#), [GPR](#), [GNN](#), [RL](#), [DSE](#), [HPO](#).

Standards and formats

Standard numbers identify families or established associations, not a claim that a listed historical edition is the latest or remains active. The table also includes related standards beyond the dictionary headword set. Consult the standards body for edition and status.

Term	Standard or owner	Guide
VHDL	IEEE 1076	R02
VHDL-AMS	IEEE 1076.1	R87
SV	IEEE 1800	R02
UVM	IEEE 1800.2	R02
UVM-MS	Accellera UVM-MS	R03
SystemC	IEEE 1666	R02 R04
SystemC AMS	IEEE 1666.1	R02 R04
UPF	IEEE 1801	R02
IP-XACT	IEEE 1685	R02
PSL	IEEE 1850	R02
SDF	IEEE 1497	R02
IP encryption	IEEE 1735	R02
PSS	Accellera PSS	R01
UCIS	Accellera UCIS	R01
SCE-MI	Accellera SCE-MI	R01
SystemRDL	Accellera SystemRDL	R01
JTAG	IEEE 1149.1	R29
Embedded core test	IEEE 1500	R28
IJTAG	IEEE 1687	R30
Three dimensional test	IEEE 1838	R31
STIL	IEEE 1450	R32
CTL	IEEE 1450.6	R32
OCI	IEEE 1450.6.1	R02
OASIS	SEMI P39	R16
IBIS and AMI	IBIS Open Forum	R39
UCle	UCle Consortium	R44
AMBA	Arm AMBA	R46
PCle	PCI SIG	R50
CXL	CXL Consortium	R51
I3C	MIPI Alliance	R49
DDR LPDDR HBM	JEDEC	R53

Primary references

Reference list reviewed on 21 October 2026 using publisher pages, bibliographic records, and public search listings. Some full standards and manuals require registration or a license. The domain index identifies the appropriate reading paths.

R01 Accellera Systems Initiative. Available Accellera standards. [Source link](#)

R02 Accellera Systems Initiative. Available IEC and IEEE standards. [Source link](#)

R03 Accellera Systems Initiative. UVM Mixed Signal standard. [Source link](#)

R04 Accellera Systems Initiative. SystemC downloads and supplemental standards. [Source link](#)

R05 Synopsys. EDA and semiconductor IP glossary. [Source link](#)

R06 Synopsys. Static timing analysis. [Source link](#)

R07 Synopsys. Power performance and area. [Source link](#)

R08 OpenROAD Project. OpenROAD implementation flow documentation. [Source link](#)

R09 OpenROAD Project. OpenSTA timing analyzer documentation. [Source link](#)

R10 OpenROAD Project. Parasitics extraction with OpenRCX. [Source link](#)

R11 OpenROAD Project. Clock tree synthesis. [Source link](#)

R12 OpenROAD Project. Global routing. [Source link](#)

R13 CIRCT Project. Circuit IR Compilers and Tools. [Source link](#)

R14 YosysHQ. Yosys synthesis documentation. [Source link](#)

R15 SMT LIB initiative. Satisfiability modulo theories background. [Source link](#)

R16 SEMI. OASIS specification SEMI P39. [Source link](#)

R17 SEMI. Compilation of Terms March 2024. [Source link](#)

R18 SkyWater PDK Project. SKY130 glossary. [Source link](#)

R19 SkyWater PDK Project. SKY130 libraries. [Source link](#)

R20 Ngspice Project. Circuit simulator documentation. [Source link](#)

R21 Ngspice Project. External compact model manuals. [Source link](#)

R22 University of California Berkeley BSIM Group. BSIM compact model family. [Source link](#)

R23 Texas Instruments. High speed analog to digital converter basics. [Source link](#)

R24 Analog Devices. Types of ADCs and DACs. [Source link](#)

R25 Cadence. Real number modeling with SystemVerilog. [Source link](#)

R26 ASML. Computational lithography. [Source link](#)

R27 ASML. Lithography lenses and mirrors. [Source link](#)

R28 IEEE Test Technology Standards Committee. Test standards projects. [Source link](#)

R29 IEEE 1149.1 Working Group. Test access port and boundary scan architecture. [Source link](#)

R30 IEEE Standards Association. IEEE 1687 embedded instrumentation access. [Source link](#)

R31 IEEE 3D Test Working Group. IEEE 1838 three dimensional test access. [Source link](#)

R32 IEEE 1450 Working Group. Standard test interface language. [Source link](#)

R33 Synopsys. Design for test. [Source link](#)

R34 Siemens. Introducing Tessent streaming scan network. [Source link](#)

R35 Siemens. Tessent IJTAG. [Source link](#)

R36 Synopsys. Electromigration. [Source link](#)

R37 Texas Instruments. Quality and reliability frequently asked questions. [Source link](#)

R38 Infineon. Failure modes effects and diagnostic analysis for AURIX. [Source link](#)

R39 IBIS Open Forum. IBIS and associated modeling standards. [Source link](#)

R40 Analog Devices. Introduction to jitter in communication systems. [Source link](#)

R41 TSMC. CoWoS packaging. [Source link](#)

R42 TSMC. Introducing the 3DFabric family. [Source link](#)

R43 Intel. EMIB technology explained. [Source link](#)

R44 UCle Consortium. About Universal Chiplet Interconnect Express. [Source link](#)

R45 Open Compute Project. Bunch of Wires PHY specification. [Source link](#)

R46 Arm. AMBA specifications. [Source link](#)

R47 Arm. CoreSight Components Technical Reference Manual DDI 0314H, Glossary, pp. Glossary-1 to Glossary-10 (PDF pages 367-376). [Source link](#)

R48 MIPI Alliance. Current specifications. [Source link](#)

R49 MIPI Alliance. I3C and I3C Basic. [Source link](#)

R50 PCI SIG. Specifications library. [Source link](#)

R51 CXL Consortium. Compute Express Link. [Source link](#)

R52 RISC V International. Ratified specifications library. [Source link](#)

R53 JEDEC. Memory and solid state technology standards. [Source link](#)

R54 Altera. HLS IP Gen Handbook, FPGA Architecture Overview. [Source link](#)

R55 AMD. Dynamic Function eXchange. [Source link](#)

R56 AMD. AXI hardware ICAP. [Source link](#)

R57 Synopsys. DSO.ai design space optimization. [Source link](#)

R58 Synopsys. VSO.ai verification space optimization. [Source link](#)

R59 Synopsys. TSO.ai test space optimization. [Source link](#)

R60 Synopsys. ASO.ai analog design optimization. [Source link](#)

R61 NVIDIA Research. DREAMPlace GPU accelerated VLSI placement. [Source link](#)

R62 Synopsys. Photonic integrated circuits. [Source link](#)

R63 Synopsys. Photonic process design kits. [Source link](#)

R64 Ansys and Synopsys. INTERCONNECT photonic circuit simulation. [Source link](#)

R65 Global Electronics Association. IPC name change announcement. [Source link](#)

R66 Boyd Kim Vandenberghe and Hassibi. A Tutorial on Geometric Programming including circuit-design applications. [Source link](#)

R67 SCIP Project. Mathematical optimization problem classes. [Source link](#)

R68 CVXPY Project. Disciplined convex programming. [Source link](#)

R69 C. Vişan, O. Pascu, M. Stănescu, E.-D. Şandru, C. Diaconu, A. Buzo, G. Pelz, and H. Cucu. Automated circuit sizing with multi-objective optimization based on differential evolution and Bayesian inference. Knowledge-Based Systems 258, 109987 (2022). [Source link](#) [Open preprint](#)

R70 SciPy Project. Optimization and root-finding methods. [Source link](#)

R71 van Ginneken and IBM Research. Buffer placement in distributed RC tree networks for minimal Elmore delay. [Source link](#)

R72 X. Zhao, Z. Bi, C. Yan, F. Yang, Y. Lu, D. Zhou, and X. Zeng. Asynchronous Batch Constrained Multi-Objective Bayesian Optimization for Analog Circuit Sizing. ASP-DAC 2024 presentation slides. [Source link](#)

R73 Lyu Yang Yan Zhou and Zeng. Batch Bayesian Optimization via Multi objective Acquisition Ensemble for Automated Analog Circuit Design. [Source link](#)

R74 Fiduccia and Mattheyses. A Linear Time Heuristic for Improving Network Partitions. [Source link](#)

R75 Kernighan and Lin. An Efficient Heuristic Procedure for Partitioning Graphs. [Source link](#)

R76 OpenROAD Project. Global placement and Nesterov optimization. [Source link](#)

R77 OpenROAD Flow Project. AutoTuner search algorithms and PPA objectives. [Source link](#)

R78 Shrestha and coauthors. Deep Representation Learning for Electronic Design Automation. [Source link](#)

R79 Scikit learn Project. Classification metrics and evaluation. [Source link](#)

R80 MIT Han Lab. GCN RL Circuit Designer and transferable transistor sizing. [Source link](#)

R81 Liu and coauthors. ChipNeMo Domain Adapted LLMs for Chip Design. [Source link](#)

R82 Z. El Sayed, Z. Wang, H. Selmani, J. Knechtel, O. Sinanoglu, and L. Alrahis. Graph Neural Networks for Integrated Circuit Design, Reliability, and Security: Survey and Tool. ACM Computing Surveys 58(4), published online 27 October 2025. [Source link](#) [Author institution record](#)

R83 Google Research. Circuit Training reinforcement learning for chip floorplanning. [Source link](#)

R84 Settaluri and coauthors. AutoCkt Deep Reinforcement Learning of Analog Circuit Designs. [Source link](#)

R85 AutoDMP authors and NVIDIA Research. Automated DREAMPlace based macro placement. [Source link](#)

R86 Boyd and Vandenberghe. Convex Optimization. [Source link](#)

R87 IEEE Standards Association. IEEE 1076.1-2017, IEEE Standard VHDL Analog and Mixed-Signal Extensions. [Source link](#)

R88 E. M. Sentovich and coauthors. SIS: A System for Sequential Circuit Synthesis. UCB/ERL M92/41 (1992). [Source link](#)

R89 Synopsys. PrimePower RTL to signoff power analysis. [Source link](#)

R90 Altera. Altera Closes Silver Lake Investment to Become World's Largest Pure-play FPGA Solutions Provider (15 September 2025). [Source link](#)

R91 Michael L. Martel and IPC. From Vacuum Tubes to Nanotubes: An Amazing Half Century. The Emergence of Electronic Circuit Technology 1957-2007 (2007). Name changes: pp. 70 and 159 (PDF pages 73 and 162). [Source link](#)

R92 Synopsys. Synopsys Introduces the HAPS-60 Series of Rapid Prototyping Systems (2010). [Source link](#)

R93 Emulation and Verification Engineering.

EVE Releases ZeBu Verification Platform for Software Developers. Press release, 4 August 2003, reproduced by Design and Reuse.

[Source link](#)

R94 Global Electronics Association. Global Electronics Association History. Official name chronology. [Source link](#)

This dictionary is intended to be extended as terminology changes. Local abbreviations should be added with an explicit domain, an example of actual use, and the governing source rather than expanded by guesswork.